Der NDR-Klein Computer

Gebrauchs- und Aufbauanleitung

F D C

ELEKTRONIKLADEN 4930 DETMOLD 18 ☎ 05232/8171

Die FDC-Karte (FDC= Floppy Disk Controller) dient zum Anschluß von Floppy Disk - Laufwerken an den NDR-Klein Computer. Es können bis zu vier Laufwerke angeschlossen werden, so daß auch große Datenmengen abgespeichert und geladen werden können.
Neben FDC-Karte und Laufwerk ist zum Betrieb natürlich noch Software erforderlich. Dies kann zunächst ein einfaches Programm wie "JOGIDOS" sein, das im 68000/ 68008-System läuft und über die Bibliotheksfunktion aufgerufen und gestartet werden kann. Die einfache Bedienung und der niedrige Preis machen dieses System besonders für den Anfänger, der erste Erfahrungen sammeln will, interessant. Für weitergehende Anforderungen sind die Betriebssysteme CP/M+ (für den Betrieb mit der Z80-CPU) und CP/M 68K und SYSTEMA-DOS (für den Betrieb mit der 68000- oder 68008-CPU) lieferbar. Diese Betriebssysteme erlauben ein komfortables Arbeiten mit Diskettenlaufwerken. Sie nehmen dem Anwender durch ihr ausgeklügeltes System viel Routinearbeit ab und beinhalten zudem wertvolle Hilfsprogramme.
Zum Betrieb der CP/M-Betriebssysteme sind mindestens 128K RAM erforderlich (ein Stück DRAM128k oder zwei Stück ROA64 mit einer ROAPROM 1 bei Z80 mit CP/M+, zwei Stück ROA-Karten oder eine DRAM128 bei 68000/68008 mit CP/M68). Außerdem wird die BANKBOOT-Karte benötigt, um dort die entsprechenden Boot-Eproms unterzubringen. (CP/M+: FLOMON (1.6 oder höher), und ELMON oder ELMON+ ;CP/M 68K: BOOT 68.)
Mit der FDC-Karte sind alle gängigen Formate möglich. Neben dem NDR-Standard 5,25", doppelte Dichte, doppelseitig, 80 Spuren, können also auch 3,5" und 8" Laufwerke, einseitig oder doppelseitig, 40 oder 80 Spuren, einfache oder doppelte Dichte behandelt werden.
In dem von uns angebotenen Gehäuse können bis zu zwei 5,25" Laufwerke integriert werden. Entsprechende Frontplatten stehen zum Gehäusebausatz zur Verfügung.

GRUNDSÄTZLICHES

Da das Aufzeichnungsverfahren der Floppy Disk relativ komplex ist, müssen wir uns zunächst einmal, wenn auch nur sehr oberflächlich, mit der Technik der Datenaufzeichnung beschäftigen. Bei der Floppy Disk handelt es sich um eine runde Scheibe (Diskette), die (ähnlich einem Tonband) eine magnetische Beschichtung trägt. Von außen nach innen verlaufen auf dieser Scheibe konzentrische Spuren (Tracks). Die Scheibe wird im Laufwerk in Drehung versetzt und der Magnetkopf des Laufwerkes, der, auf einem beweglichen Arm montiert, vor und zurück bewegt werden kann, kann einzelne Spuren anfahren und dort entweder Daten schreiben oder dort gespeicherte Daten lesen.

Jede Spur ist in mehrere Sektoren unterteilt, von denen jeder genau die gleiche Menge an Daten enthält. So kann der Magnetkopf des Laufwerkes, wenn ihm die Informationen über Spur und Sektor der gesuchten Daten angegeben wird, diese Stelle anfahren und die dort gespeicherten Daten lesen, oder an genau dieser Stelle Daten schreiben. Die Kennung der Spuren und der Sektoren ist auf der Diskette abgespeichert. Dieses Verfahren, bei dem die Kennungen auf der Diskette gespeichert sind, nennt man "Soft-Sektorierung". Noch vor einigen Jahren gab es dagegen die so genannte "Hard-Sektorierung, bei dem der Sektor über einen Kreis kleiner um das Zentrum der Diskette angebrachter Löcher abgefragt wurde.
Die Daten werden vom FDC sequentiell zum Laufwerk übertragen. Da sich die Diskette aber bei der Datenwiedergabe nie genau so schnell dreht wie beim Beschreiben des jeweiligen Sektors, wird zusammen mit den zu speichernden Daten auch eine Information über den Datentakt übertragen. Bei der Wiedergabe der Daten werden diese in ein Schieberegister geladen und dieses Register dann mit dem rückerhaltenen Takt betrieben.
Das Aufzeichnungsverfahren, das wir bei der FDC-Karte benutzen heißt MFM (Modified Frequenzy Modulation). Es erlaubt, die Diskette in sogenannter doppelter Schreibdichte (double density) zu beschreiben.

SCHALTUNGSBESCHREIBUNG

Zentraler Chip auf der FDC-Karte ist der integrierte Baustein FDC 1797 (IC 5), der Controller-Chip. Es handelt sich hier um einen intelligenten Prozessor, der alle logischen und verwaltungstechnischen Aufgaben auf der FDC-Karte erledigt. Er besitzt unter anderem den Befehl "Lies Spur", mit dem eine Spur auf der Diskette vollständig gelesen werden kann. Er sucht und findet auf Anforderung die richtige Spur, meldet das Ergebnis an die CPU und liefert die angeforderten Daten dort ab. Da der FDC ein hochkomplexer Chip ist, haben wir im "Hintergrund" das Wichtigste aus dem Datenblatt abgedruckt. Hier finden Sie eine Auflistung der "integrierten Befehle":

Typ	Befehl	7	6	5	4	3	2	1	0
I	Restore / Auf Spur 0 /	0	0	0	0	h	V	R0	R1
I	Seek / Spur suchen /	0	0	0	1	h	V	R0	R1
I	Step / schreiten /	0	0	1	u	h	V	R0	R1
I	Step in /schreite nach Innen	0	1	0	u	h	V	R0	R1
I	Step out/schreite nach Außen	0	1	1	u	h	V	R0	R1
II	Read Sektor/ Lese Sektor	1	0	0	m	F2	E	F1	0
II	Write Sektor/ Schreibe Sekt.	1	0	1	m	F2	E	F1	a0
III	Read Address/ Lese Adresse	1	1	0	0	0	E	F1	0
III	Read Track / Lese Spur	1	1	1	0	0	E	F1	0
III	Write Track/ Schreibe Spur	1	1	1	1	0	E	F1	0
IV	Force Interrupt/ I. auslösen	1	1	0	1	I3	I2	I1	I0

Zwischen dem FDC 1797 und dem Laufwerk steht der Datenseperator FDC 9229B (IC 7). Die Aufgabe des Datenseperators ist es, die Schreib- und Lesesignale des 1797 so aufzubereiten, daß sie von der Elektronik des Laufwerkes verstanden werden können. Darüberhinaus trennt (separiert) er auch beim Lesevorgang die vorher zugegebenen Synchronisations-Signale von den Datenbits. Neben dem Datenseparator enthält der 9229 auch die Schaltung für die Präkompensation.

Da es auf den inneren Spuren einer Diskette zu einer Impulsverschiebung der gelesenen gegenüber der vorher geschriebenen Daten kommt, ist eine solche Präkompensation häufig notwendig. Ob für die von Ihnen verwendeten Laufwerke eine Präkompensation notwenig ist, finden Sie in den Unterlagen zum Laufwerk. Zur Einstellung der Präkompensationszeit verfügt der 9229 über die Eingänge P0, P1 und P2.
Für 5,25"- oder 3,5" Laufwerke ergibt sich folgende Beschaltungsmöglichkeit, die auf der FDC-Karte durch das Stecken der Jumper im Feld ST5 realisiert werden (siehe auch Seite 6):

Brücken						P 2	P 1	P0	
A	B	C	D	E	F				
			X	X	X	L	L	L	0 ns
		X	X	X		L	L	H	125 ns
	X		X		X	L	H	L	150 ns
	X	X	X			L	H	H	375 ns
X		X		X		H	L	L	500 ns
X	X				X	H	L	H	500 ns
X	X	X				H	H	L	625 ns
						H	H	H	625 ns

X = Jumper gesteckt

Der auf der FDC-Karte eingestzte PAL-Baustein 10H8 übernimmt auf der Karte die Adreßdekodierung.
Die FDC-Karte belegt die Adressen C0h - C7h. Darüber hinaus erzeugt der PAL-Baustein zusammen mit dem 74LS164 (IC12 <Schieberegister>) die Waitzyklen, die über Steckbrücken im Feld ST7 einstellbar sind.
Die von der CPU über den Bus kommenden Daten (Bus-Pins 8 - 15) werdem im 74LS374 (IC 4 <Latch>) zwischengespeichert und an den Controller 1797 weitergegeben. Wenn Daten von der FDC zur CPU gegeben werden, gehen diese Daten zum 74LS367 (IC2 <Treiber>) und einem Teil des zweiten 74LS367 (IC3). Die 6 Datenbits gehen über IC2, die restlichen 2 Bits gehen über IC3 und gelangen von dort auf den Bus. Die hierbei nicht genutzten Treiberkanäle von IC3 übermitteln die Statussignale der FDC über Port C4h an die CPU.

Der 74LS273 (IC1 <Latch>) dient als Zwischenspeicher für dieses Steuerport. Die Software gibt die entsprechenden Information an diesen Baustein, der dann das Laufwerk (die Laufwerke) anspricht.

Die Bedeutung der Bits in Port C4h beim Schreibvorgang:

```
7   6   5   4   3   2   1   0
:   :   :   :   :   :   :   :
:   :   :   :   :...:...:...:. L a u f w e r k
:   :   :   :                  D   C   B   A
:   :   :   :                  1 = Laufwerk an
:   :   :   :
:   :   :   :.................. 1 = einfache Dichte (sd)
:   :   :                      0 = doppelte Dichte (dd)
:   :   :
:   :   :..................... 1 = Mini Floppy
:   :                          0 = Maxi Floppy
:   :
:   :......................... 1 = Motor aus
:                              0 = Motor an
:
:........................... 1 = Seite 1
                               0 = Seite 0
```

Die Bedeutung der Bits in Port C4h beim Lesevorgang

```
7   6   5   4   3   2   1   0
:  INT  :   :   x   x   x   x
DRQ : Headld:
:   :   :   :.................. 1 = Kein zweiseitiges Laufwerk
:   :   :                      0 = zweiseitiges Laufwerk
:   :   :
:   :   :..................... 1 = Kopf liegt auf Diskette
:   :                          0 = Kopf liegt nicht auf
:   :
:   :......................... 1 = 1797-Intrq liegt an (*)
:                              0 = kein Intrq
:
:........................... 1 = Daten-Request liegt an
                               0 = kein DRQ
```

(*) Interrupt-Request

Die beiden Schaltungen 74LS540 und 74LS541 (IC6, 8 <Leitungstreiber>) treiben die Informationen vom Controller (1797) zu den Laufwerken, bzw. von den Laufwerken zum Controller-Chip.

Die Schaltungsergänzung (Seite 10)zeigt zwei Monoflops. Das erste Monoflop wird von Motor-on-Signal angestoßen und gibt (,wenn Jumper auf Stellung B-C steckt) einen 20-Sekunden-Impuls ab. Nach 20 Sekunden wird so, wenn nicht in der Zwischenzeit wieder auf das Laufwerk zugegriffen wird, der Motor des Laufwerkes abgeschaltet. Wenn der Jumper in Stellung A - B steckt läuft der Motor bis der Software-Befehl "Motor aus" kommt.
Das zweite Monoflop erzeugt ein Ready-Signal, was bei Laufwerken nötig ist, die dieses Signal nicht von sich aus liefern. Die gesamte Quarzoszillatorschaltung, die auf den anderen Karten aus einem Quarz und einigen Widerständen besteht, befindet sich hier im Gehäuse des Quarzoszillatore (OSZ), der die benötigten 16 MHz liefert.

Im folgenden finden Sie die Belegung der Steckfelder auf der FDC-Karte. Die Belegung des Feldes ST5 (Präkompensation) finden Sie im Text auf Seite 4.

	A - B gesteckt	B - C gesteckt
ST1	Sideselect durch Software(*)	Sideselect vom 1797
ST2	Motor dauernd an	Motor On durch Software(*)
ST8	INT-Leitung mit Bus verb.	
ST10	Driveselect mit Headlaod	Driveselect ohne Headload
ST11	Motor On ohne Monoflop	Motor On über Monoflop
ST12	Ready vom Monoflop	Ready vom Laufwerk

(*)

ST1 und ST2 sind auf der FDC-Karte bereits auf die die mit * gekennzeichneten Postitionen vorgeätzt.

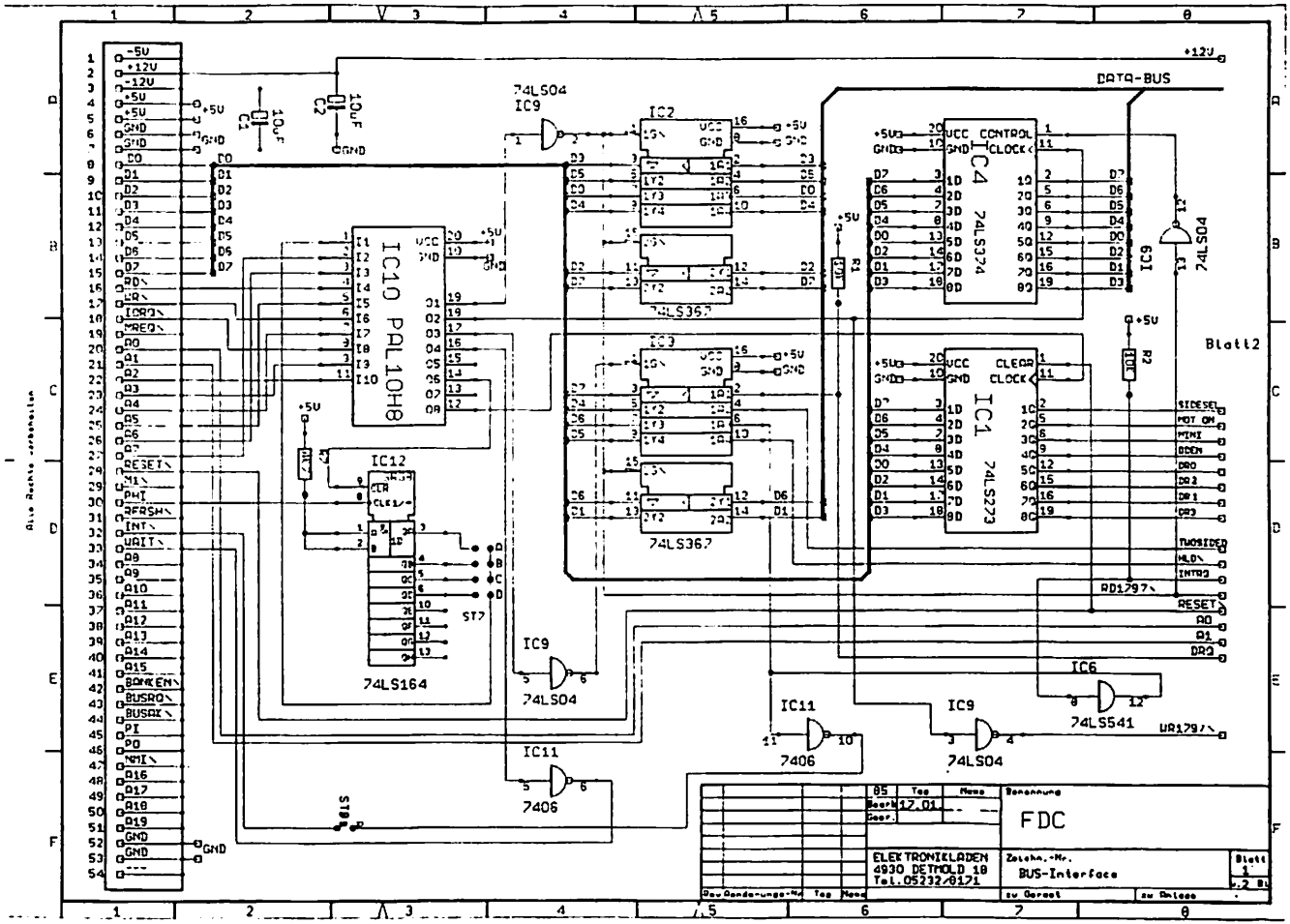
ST7 Anzahl der Waitzyklen für den 68008.
Keine Brücke gesteckt: kein Waitzyklus
Brücke A gesteckt : 1 Waitzyklus
Brücke B gesteckt : 2 Waitzyklen
Brücke C gesteckt : 3 Waitzyklen
Brücke D gesteckt : 4 Waitzyklen

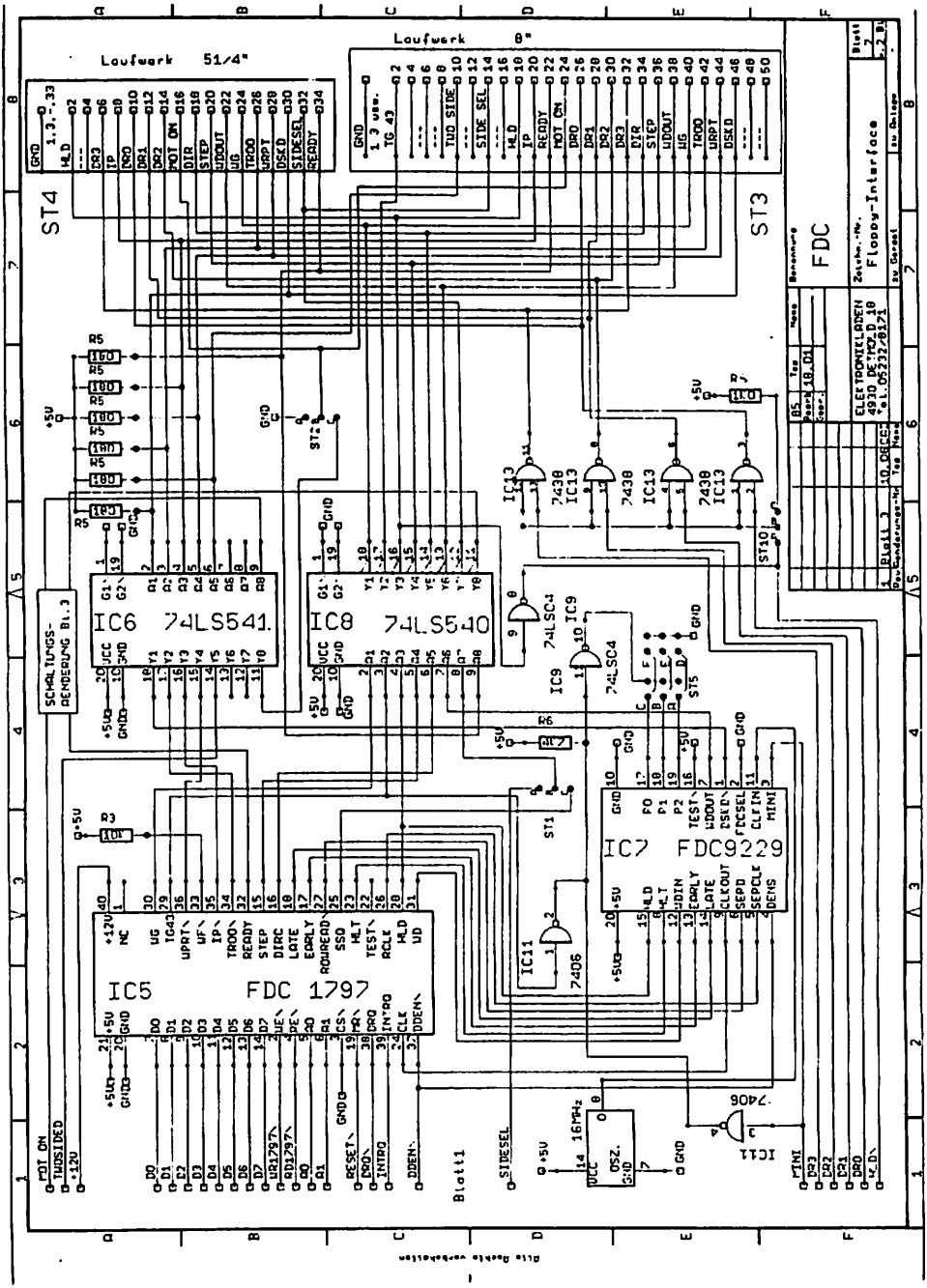
	CP/M 2.2	CP/M+	CP/M68K
ST8	gesteckt	offen	offen
ST10	A-B gesteckt	B-C gesteckt	A-B gesteckt
ST11	A-B gesteckt	B-C gesteckt	A-B gesteckt

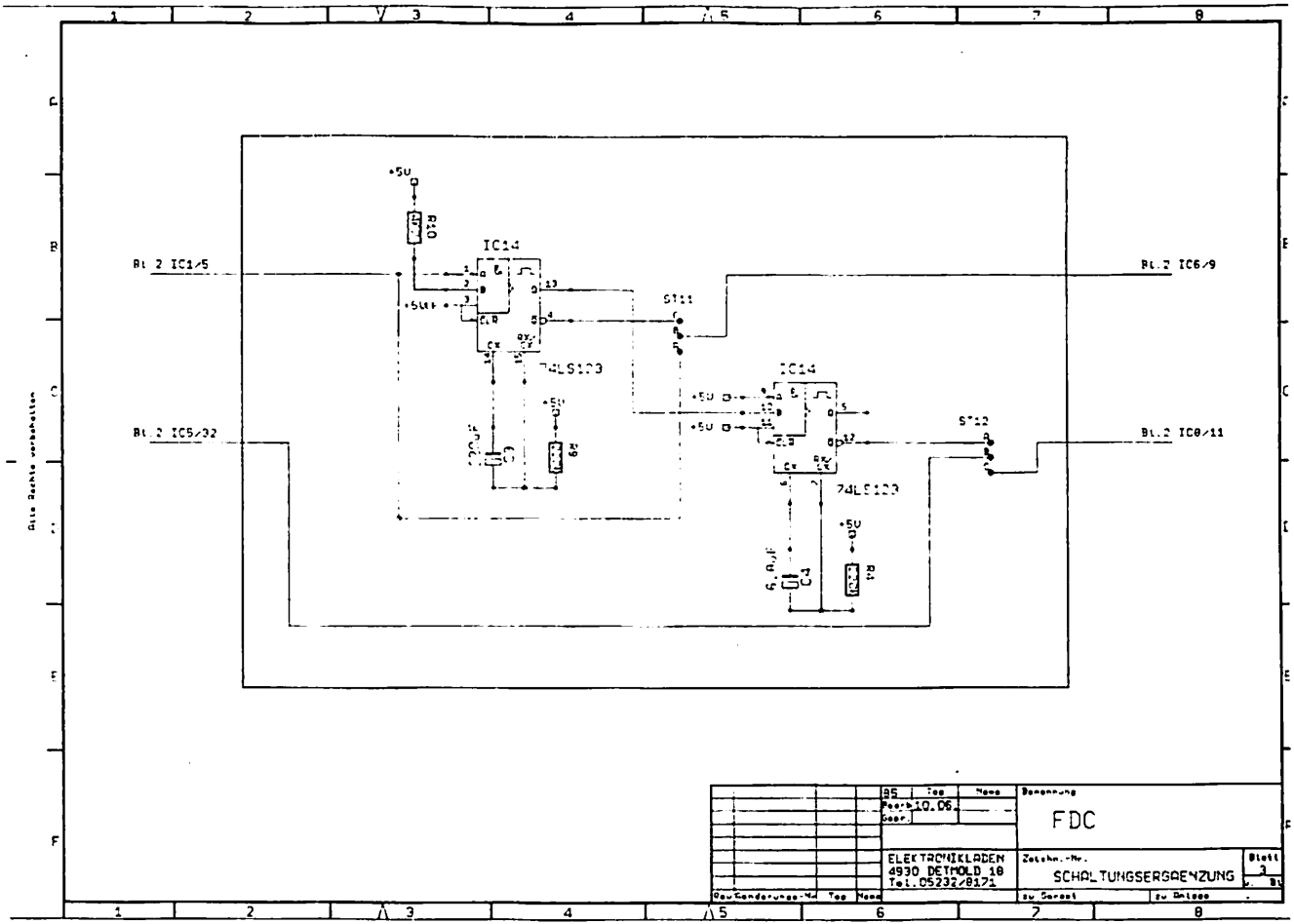
ST12 A-B muß gesteckt sein, beim Einsatz von Laufwerken, die kein Ready-Signal liefern.
B-C muß gesteckt sein, beim Einsatz von Laufwerken, die ein Ready-Signal liefern.

Die Belegung der Steckerleisten ST3 und ST4 finden Sie im Schaltplan auf Seite 9.

Beachten Sie bitte, daß bei diesen Steckerleisten alle Pins mit ungeraden Nummern auf Masse liegen.


DATA-BUS
+12V
-5V
+5V
GND
IC10 PAL10H8
74LS164
74LS374
74LS373
74LS367
74LS04
74LS541
7406
IC1
IC2
IC3
IC4
IC6
IC9
IC11
IC12
Blatt2
FDC
ELEKTRONIKLADEN
4930 DETMOLD 10
Tel.05232/0171
BUS-Interface

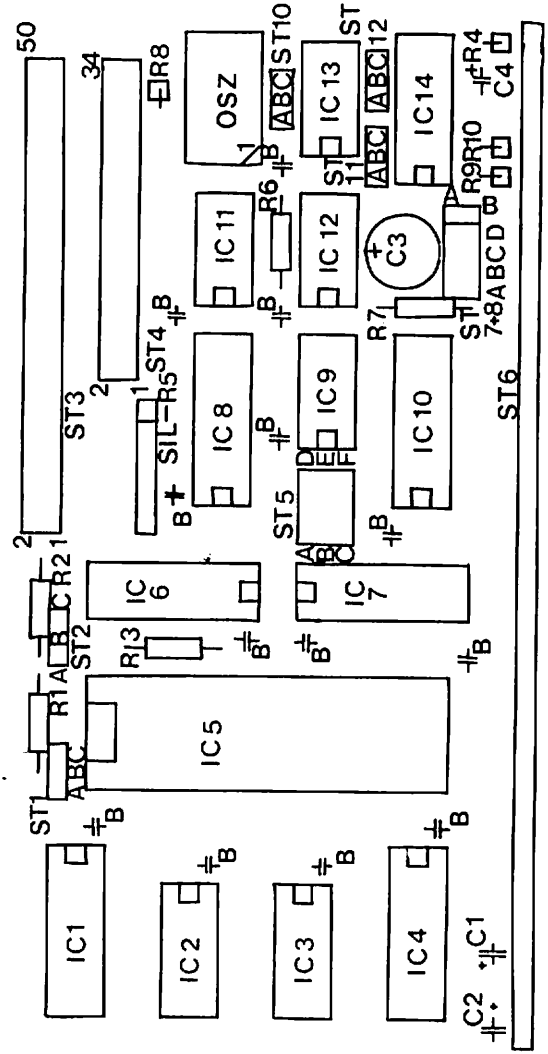

Laufwerk 51/4"
Laufwerk 8"
ST4
ST3
FDC
IC5 FDC 1797
IC6 74LS541
IC8 74LS540
IC7 FDC9229
IC9 74LSC04
IC11 7406
IC13 7438
Floppy-Interface
Blatt1


Bl.2 IC1/5
Bl.2 IC5/12
Bl.2 IC6/9
Bl.2 IC8/11
IC14
74LS123
ST11
ST12
+5U
R10
R9
C3
C4
6,8µF
0,1µF
Alle Rechte vorbehalten
ELEKTRONIKLADEN
4930 DETMOLD 18
Tel.05232/8171
Bezeichnung
FDC
SCHALTUNGSERGAENZUNG
Blatt 1

STÜCKLISTE

Stück	Aufdruck	Beschreibung
1	IC 1	Int. Schaltung 74LS273
2	IC 2, 3	Int. Schaltung 74LS367
1	IC 4	Int. Schaltung 74LS374
1	IC 5	Int. Schaltung FDC 1797
1	IC 6	Int. Schaltung 74LS541
1	IC 7	Int. Schaltung FDC 9229B
1	IC 8	Int. Schaltung 74LS540
1	IC 9	Int. Schaltung 74LS04
1	IC 10	Int. Schaltung PAL10H8
1	IC 11	Int. Schaltung 7406
1	IC 12	Int. Schaltung 74LS164
1	IC 13	Int. Schaltung 7438
1	IC 14	Int. Schaltung 74LS123
1	OSZ	Quarzoszillator 16MHz
13	B	Keram. Kondensator 100nF
2	C 1, 2	Tantal Elko 10uF/16V
1	C 3	Elko 220uF/16V
1	C 4	Tantal Elko 6,8uF/16V
3	R 1, 2, 3	Widerstand 10 kOhm
2	R 4, 9	Widerstand 220 kOhm
3	R 6, 7, 10	Widerstand 4,7 kOhm
1	R 8	Widerstand 1 kOhm
1	SIL-R5	Widerstands Array 6 x 180 Ohm
4	zu IC 9, 11, 12, 13	IC-Sockel DIL 14
3	zu IC 2, 3, 14	IC-Sockel DIL 16
6	zu IC 1, 4, 6, 7, 8, 10	IC-Sockel DIL 20
1	zu IC 5	IC-Sockel DIL 40
3	ST 10, 11, 12,	Stiftleiste 1 x 3pin
1	ST 3	Stiftleiste 2 x 25pin
1	ST 4	Stiftleiste 2 x 17pin
1	ST 5	Stiftleiste 3 x 4pin
1	ST 6	Stiftleiste 54pin abgew.
1	ST 7, 8	Stiftleiste 2 x 5pin
8		Jumper
1		Leiterplatte

BESTÜCKUNGSDRUCK



BESTÜCKUNG

Wie bei allen Karten beginnen Sie auch hier bitte zuerst mit der Bestückung der passiven Bauteile und der Stiftleiste ST6, die die FDC-Karte mit dem Bus verbindet. Achten Sie auch bei dieser Karte darauf, daß alle Pins des Steckers parallel zur Karte ausgerichtet sind, bevor Sie mit dem Löten beginnen. Als nächstes löten Sie alle im Bestückungsdruck mit "B" bezeichneten Keramikkondensatoren ein. Jetzt winkeln Sie die Widerstände R1, R2, R3 (10 KOhm), R6 und R7 (4,7 KOhm) ab und löten Sie diese Widerstände ein. Sie werden liegend eingelötet. Alle anderen Widerstände, die Sie als nächstes einlöten werden stehend eingelötet. Als letzen "Widerstand" montieren Sie nun das Netzwerk SILR5. Das Netzwerk hat an einem Ende einen Punkt. Es kennzeichnet den gemeinsamen Pol der 6 Widerstände, die das Netzwerk integriert. Im Bestückungsdruck finden Sie ein kleines Quadrat. Dieses Quadrat kennzeichnet den Lötpunkt, in den dieser gemeinsame Pol eingelötet wird. Jetzt sind die Elektrolytkondensatoren "an der Reihe". Sie finden zwei Formen von "Elkos": Tantals (C1, 2 und 4) und einen "echten Elko" (C3). Alle diese Kondensatoren sind gepolt. Seien Sie also hier sehr sorgfältig. Sie finden im Bestückungsdruck der Kondensatoren ein "+"-Zeichen. Es markiert den Plus-Pol. Auf den Tantals finden Sie den Pluspol mit einem kleinen "+" gekennzeichnet. Bei C3, dem stehenden Alu-Elko ist der Minus-Pol mit einem "-"-Zeichen gekennzeichnet. Fertigen Sie nun aus den im Bausatz mitgelieferten Steckerleisten die erforderlichen Steckleisten zusammen. Achten Sie aber dareuf, daß ST1 und ST2 vorgeätzt sind. Diese beiden Stecker werden also NICHT bestückt. Die Reihen ST10 (3pol), ST11 (3pol) und ST12 (3pol) sind einreihig, die Steckerleisten ST3 (2x25), ST4 (2x17), ST7,8 (2x5) sind zweireihig, das Rasterfeld ST5 besteht aus 3 Stück 4poligen Reihen. Die Steckerleisten lassen sich ohne Schwierigkeit parallel aneinanderreihen, da sie kleine Kunststoffnoppen haben, die bei Druck einrasten und so mehrreihige Leisten schaffen.
Wenn Sie diese Steckerreihen eingelötet haben, beginnen Sie mit dem Einbau der IC-Fassungen und des Quarzoszillators. Dem Punkt, den Sie an einer Ecke des Metallgehäuses am Oszillator finden, entspricht das kleine Dreieck (mit den Pin 1), das Sie im Bestückungsdruck (OSZ) sehen. Bei allen IC-Positionen im Bestückungsdruck finden Sie die "Richtung" des ICs durch ein kleines Viereck gekennzeichnet.
Löten Sie bitte die IC-Fassungen so ein, daß die Kennzeichnung, die die Fassung trägt in die gleiche Richung weist, in die auch dieses Viereck "schaut". In der gleichen Richtung sollen später die integrierten Schaltungen eingesteckt werden, die alle zur

Markierung ein Kerbe tragen (nicht der eingeprägte Kreis, der kennzeichnet PIN1). Gehen Sie beim Einlöten der Fassungen sowie beim folgenden Einstecken der ICs bitte langsam und sorgfältig vor, denn beim Anlegen der Spannung werden falsch herum eingesteckte ICs sofort (meist) zerstört.
Kontrollieren Sie nun, da die Karte vollständig bestückt ist mit einer Lupe alle Lötstellen auf der Lötseite. "Kalte" Lötstellen können Ihnen die Freude an der FDC-Karte nachhaltig verderben. Löten Sie daher alle Ihnen "verdächtig" erscheinenden Stellen noch einmal nach. Kontrollieren Sie auch, ob alle ICs auf der Bestückungsseite richtig stecken. Manchmal wird beim Einstecken ein Pin abgeknickt. Mit einer Lupe werden Sie diese Fehler jedoch sicherlich finden.
Kontrollieren Sie noch einmal, daß Sie ST1 und ST2, die vorgeätzt sind, nicht bestückt haben. Die "Nasen" (also die Kerben) von IC 5 und IC 6 weisen aufeinander. Die Nasen der ICs 1 - 4 weisen nach rechts, die der ICs 10 - 14 nach links. Wenn das bei Ihnen so ist, stecken alle ICs richtig.
Jetzt ist die Karte "funktionsfähig" aufgebaut. Wenn kein Fehler vorliegt, funktioniert sie jetzt auch wunschgemäß.

HÄUFIGE FEHLER:

1. Die FDC-Karte benötigt neben +5V auch +12V. Diese +12V müssen am Pin2 des Busses vorhanden sein.
2. Jumper werden falsch gesteckt. Beachten Sie unbedingt die Tabellen auf den Seiten 4 und 7.
3. ST1 und ST2 sind vorgeätzt. Sie werden nicht bestückt.
4. Lesen Sie (vor dem Anschluß) sorgfältig die Unterlagen der Floppy-Disk-Laufwerke (Abschlußbelegung!). Wenn Sie mehrere Laufwerke anschließen, müßen Sie bei allen -außer einem- ein Widerstansarray entfernen, das meist in der Nähe des Kabelanschlusses steckt. Das Array kann wie ein IC aussehen (zB. bei Mitsubishi 5 1/4" Laufwerken).
   Auf jedem Laufwerk muß der Drive-Select-Jumper (DS) richtig stecken (DS0 = Laufwerk A, DS1 = Laufwerk B, usw.) Beachten Sie die Unterlagen, die Sie mit den Laufwerken erhalten.

Wenn Sie Schwierigkeiten bei der Erstellung der benötigten Kabel haben, bedenken Sie, daß Sie Kabel fertige Kabel von uns beziehen können. "Hinfummeln" kann hier schlimme Folgen haben!

ACHTUNG:

Bei Verwendung von Laufwerken des Fabrikats TEAC (z.B. FD55) ist es sinnvoll folgende Änderung vorzunehmen:

Trennen Sie an ST2 die Verbindung B - C auf.

Verbinden Sie nun Pin B von ST2 mit Pin2 von ST4.

Nun wird der Motor des Laufwerkes sich nach jedem Zugriff abschalten und nicht ständig laufen.

STANDARD MICROSYSTEMS CORPORATION

FDC 1791-02
FDC 1792-02
FDC 1793-02
FDC 1794-02
FDC 1795-02
FDC 1797-02

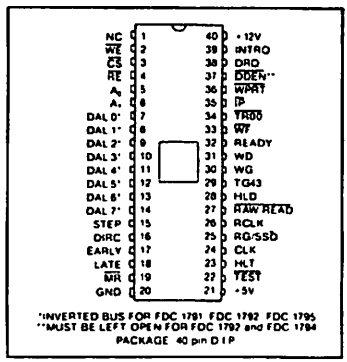
Floppy Disk Controller/Formatter FDC

μPC FAMILY

FEATURES

- ☐ SOFT SECTOR FORMAT COMPATIBILITY
- ☐ AUTOMATIC TRACK SEEK WITH VERIFICATION
- ☐ ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
  - IBM 3740 Single Density (FM)
  - IBM System 34 Double Density (MFM)
- ☐ READ MODE
  - Single/Multiple Sector Read with Automatic Search or Entire Track Read
  - Selectable 128 Byte or Variable Length Record
- ☐ WRITE MODE
  - Single/Multiple Sector Write with Automatic Sector Search
  - Entire Track Write for Diskette Initialization
- ☐ PROGRAMMABLE CONTROLS
  - Selectable Track to Track Stepping Time
  - Side Select Compare
- ☐ SYSTEM COMPATIBILITY
  - Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
  - DMA or Programmed Data Transfers
  - All Inputs and Outputs are TTL Compatible
  - On-chip Track and Sector Registers/Comprehensive Status Information
- ☐ WRITE PRECOMPENSATION (MFM AND FM)
- ☐ SIDE SELECT LOGIC (FDC 1795, FDC 1797)
- ☐ WINDOW EXTENSION (IN MFM)

PIN CONFIGURATION



- ☐ INCORPORATES ENCODING/DECODING AND ADDRESS MARK CIRCUITRY
- ☐ COMPATIBLE WITH FD179X-02
- ☐ COPLAMOS® n-CHANNEL MOS TECHNOLOGY
- ☐ COMPATIBLE WITH THE FDC 9216 FLOPPY DISK DATA SEPARATOR

GENERAL DESCRIPTION

The FDC 179X is an MOS/LSI device which performs the functions of a Floppy Disk Controller/Formatter in a single chip implementation. The basic FDC 179X chip design has evolved into six specific parts: FDC 1791, FDC 1792, FDC 1793, FDC 1794, FDC 1795, and the FDC 1797.

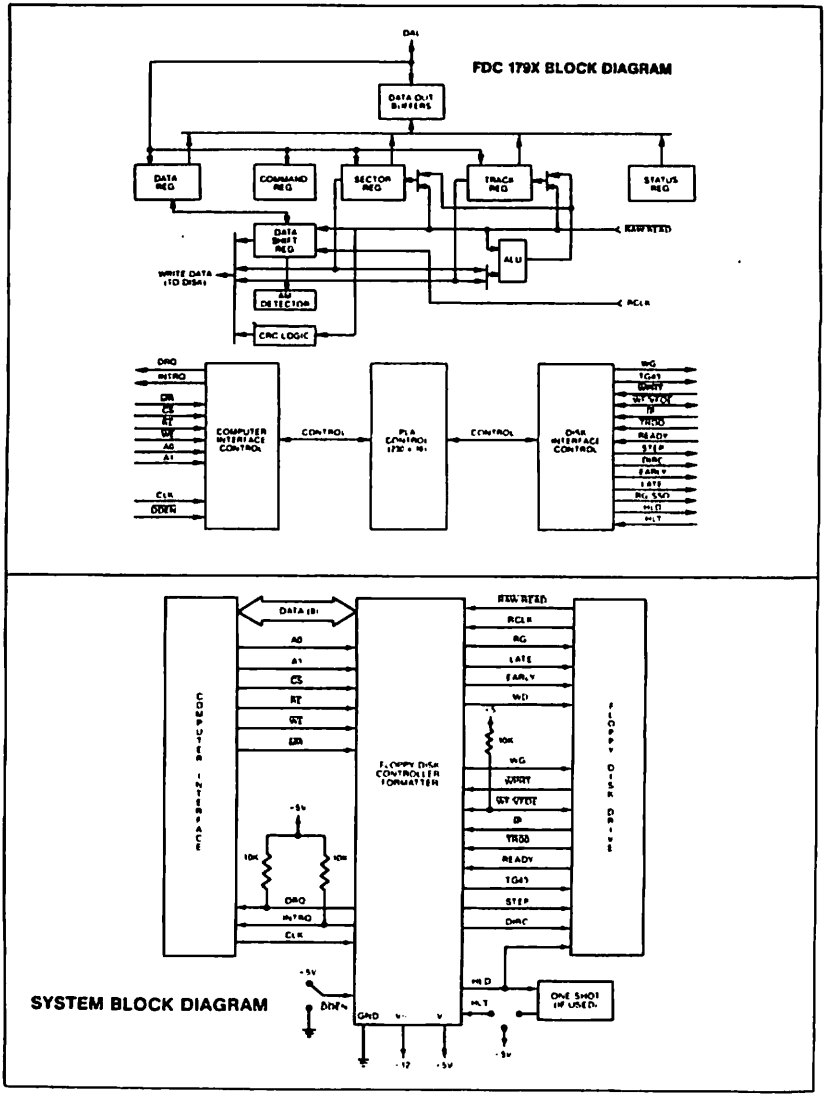
This FDC family performs all the functions necessary to read or write data to any type of floppy disk drive. Both 8" and 5¼" (mini-floppy) drives with single or double density storage capabilities are supported. These n-channel MOS/LSI devices will replace a large amount of discrete logic required for interfacing a host processor to a floppy disk.

The FDC 1791 is IBM 3740 compatible in single density mode (FM) and System 34 compatible in double density mode (MFM). The FDC 1791 contains enhanced features necessary to read/write and format a double density diskette. These include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation.

The FDC 1793 is identical to the FDC 1791 except the DAL lines are TRUE for systems that utilize true data busses.

The FDC 1792 operates in the single density mode only. Pin 37 (DDEN) of the FDC 1792 must be left open for proper operation. The FDC 1794 is identical to the FDC 1792 except the DAL lines are TRUE for systems that utilize true data busses. The FDC 1795 adds side select logic to the FDC 1791. The FDC 1797 adds the side select logic to the FDC 1793.

The processor interface consists of an 8 bit bidirectional bus for data, status, and control word transfers. This family of controllers is configured to operate on multiplexed bus with other bus-oriented devices.


FDC 179X BLOCK DIAGRAM
DATA OUT BUFFERS
DATA REG
COMMAND REG
SECTOR REG
TRACK REG
STATUS REG
DATA SHIFT REG
ALU
WRITE DATA (TO DISK)
A.M. DETECTION
CRC LOGIC
COMPUTER INTERFACE CONTROL
CONTROL
PLA CONTROL
DISK INTERFACE CONTROL
DRQ
INTRQ
CLK
DDEN
COMPUTER INTERFACE
FLOPPY DISK CONTROLLER FORMATTER
FLOPPY DISK DRIVE
SYSTEM BLOCK DIAGRAM
ONE SHOT (IF USED)

DESCRIPTION OF PIN FUNCTIONS

PIN NO	NAME	SYMBOL	FUNCTION
1	NO CONNECTION	NC	This pin is internally connected to the substrate bias generator and must be left open
20	GROUND	V_{ss}	Ground
21	POWER SUPPLY	V_{cc}	+5V
40	POWER SUPPLY	V_{DD}	+12V
19	MASTER RESET	$\overline{MR}$	A logic low on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during $\overline{MR}$ ACTIVE. When $\overline{MR}$ is brought to a logic high a Restore Command is executed regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into the sector register
COMPUTER INTERFACE:			
2	WRITE ENABLE	$\overline{WE}$	A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low
3	CHIP SELECT	$\overline{CS}$	A logic low on this input selects the chip and the parallel data bus (DAL)
4	READ ENABLE	$\overline{RE}$	A logic low on this input controls the placement of data from a selected register on DAL0-DAL7 when $\overline{CS}$ is low
5,6	REGISTER SELECT LINES	A0 A1	These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control A1 | A0 | $\overline{RE}$ | $\overline{WE}$ 0 | 0 | Status Reg | Command Reg 0 | 1 | Track Reg | Track Reg 1 | 0 | Sector Reg | Sector Reg 1 | 1 | Data Reg | Data Reg
7-14	DATA ACCESS LINES	DAL0-DAL7	Eight bit Bidirectional bus used for transfer of data, control and status. This bus is a receiver enabled by $\overline{WE}$ or a transmitter enabled by $\overline{RE}$. The Data Bus is inverted on the FDC 1791, FDC 1792 and FDC 1795
24	CLOCK	CLK	This input requires a free-running square wave clock for internal timing reference. 2 MHz for 8" drives, 1 MHz for 5¼" drives
38	DATA REQUEST	DRQ	This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operations respectively. Use a 10K pull-up resistor to +5V
39	INTERRUPT REQUEST	INTRQ	This open drain output is set at the completion or termination of any operation and is reset when a new command is loaded into the command register or the status register is read. Use a 10K pull-up resistor to +5V
FLOPPY DISK INTERFACE:			
15	STEP	STEP	Step and direction motor control. The step output contains a pulse for each step
16	DIRECTION	DIRC	Direction Output is active high when stepping in, active low when stepping out
17	EARLY	EARLY	Indicates that the write data pulse occurring while Early is active (high) should be shifted early for write precompensation
18	LATE	LATE	Indicates that the write data pulse occurring while Late is active (high) should be shifted late for write precompensation
22	TEST	TEST	This input is used for testing purposes only and should be tied to +5V or left open by the user unless interfacing to voice coil actuated motors
23	HEAD LOAD TIMING	HLT	When a logic high is found on the HLT input the head is assumed to be engaged

PIN NO.	NAME	SYMBOL	FUNCTION
25	READ GATE (1791/3)	RG	A high level on this output indicates to the data separator circuitry that a field of zeros (or ones) has been encountered and is used for synchronization
25	SIDE SELECT OUTPUT (1795, 1797)	SSO	The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When S = 1, SSO is set to a logic 1. When S = 0, SSO is set to a logic 0. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition
26	READ CLOCK	RCLK	A nominal square-wave clock signal derived from the data stream must be provided to this input. Phasing (i.e. RCLK transitions) relative to RAW READ is important but polarity (RCLK high or low) is not
27	$\overline{\text{RAW READ}}$	$\overline{\text{RAW READ}}$	The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media
29	TRACK GREATER THAN 43	TG43	This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands
30	WRITE GATE	WG	This output is made valid before writing is to be performed on the diskette
31	WRITE DATA	WD	A 250 ns (MFM) or 500 ns (FM) pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats
32	READY	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7
33	$\overline{\text{WRITE FAULT}}$/ $\overline{\text{VFO ENABLE}}$	$\overline{\text{WF/VFOE}}$	This is a bi-directional signal used to signify writing faults at the drive, and to enable the external PLO data separator. When WG = 1, Pin 33 functions as a $\overline{\text{WF}}$ input. If $\overline{\text{WF}}$ = 0, any write command will immediately be terminated. When WG = 0, Pin 33 functions as a $\overline{\text{VFOE}}$ output. $\overline{\text{VFOE}}$ will go low during a read operation after the head has loaded and settled (HLT = 1). On the 1795/7, it will remain low until the last bit of the second CRC byte in the ID field. $\overline{\text{VFOE}}$ will then go high until 8 bytes (MFM) or 4 bytes (FM) before the Address Mark. It will then go active until the last bit of the second CRC byte of the Data Field. On the 1791/3, $\overline{\text{VFOE}}$ will remain low until the end of the Data Field
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	This input informs the FDC179X that the Read/Write head is positioned over Track 00
35	$\overline{\text{INDEX PULSE}}$	$\overline{\text{IP}}$	This input informs the FDC179X when the index hole is encountered on the diskette
36	$\overline{\text{WRITE PROTECT}}$	$\overline{\text{WPRT}}$	This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit
37	$\overline{\text{DOUBLE DENSITY}}$	$\overline{\text{DDEN}}$	This pin selects either single or double density operation. When $\overline{\text{DDEN}}$ = 0, double density is selected. When $\overline{\text{DDEN}}$ = 1, single density is selected. This line must be left open on the 1792/4

FUNCTIONAL DESCRIPTION

The FDC 179X-02 major functional blocks are as follows:

Data Shift Register—This 8-bit register assembles serial data from the Read Data input ($\overline{\text{RAW READ}}$) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register—This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Sector Register (SR)—This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR)—This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a Force Interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR)—This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic—This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

Track Register—This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU)—The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control—All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

AM Detector—The address mark detector detects ID, data and Index address marks during ready and write operations.

OPERATION

FDC 1791, FDC 1793, FDC 1795 and FDC 1797 have two modes of operation according to the state of $\overline{\text{DDEN}}$ (Pin 37). When $\overline{\text{DDEN}} = 1$, single density is selected. In either case, the CLK input (Pin 24) is at 2 MHz. However, when interfacing with the mini-floppy, the CLK input is set at 1 MHz for both single density and double density. When the clock is at 2 MHz, the stepping rates of 3, 6, 10, and 15 ms are obtainable. When CLK equals 1 MHz these times are doubled.

DDEN must be left open for the FDC 1792 and FDC 1794.

Disk Read Operation

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{\text{DDEN}}$ should be placed to logical "1." For MFM formats, $\overline{\text{DDEN}}$ should be placed to a logical "0." Sector lengths are determined at format time by a special byte in the "ID" field. If this Sector length byte in the ID field is zero, then the sector length is 128 bytes. If 01 then 256 bytes. If 02, then 512 bytes. If 03, then the sector length is 1024 bytes. The number of sectors per track can be from 1 to 255 sectors. The number of tracks is from 0 to 255 tracks.

For read operations, the FDC 179X requires $\overline{\text{RAW READ}}$ Data (Pin 27) signal which is a 250 ns pulse per flux transition and a Read clock (RCLK) signal to indicate flux transition spacings. The RCLK (Pin 26) signal is provided by some drives but if not, it may be derived externally by Phase lock loops, one shots, or counter techniques. In addition, a Read Gate Signal is provided as an output (Pin 25) which can be used to inform phase lock loops when to acquire synchronization. When reading from the media in FM, RG is made true when 2 bytes of zeroes are detected. The FDC179X must find an address mark within the next 10 bytes, otherwise RG is reset and the search for 2 bytes of zeroes begins all over again. If an address mark is found within 10 bytes, RG remains true as long as the FDC179X is deriving any useful information from the data stream. Similarly for MFM, RG is made active when 4 bytes of "00" or "FF" are detected. The FDC179X must find an address mark within the next 16 bytes, otherwise RG is reset and search resumes.

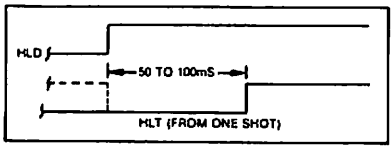
During read operations (WG = 0), the $\overline{\text{VFOE}}$ (Pin 33) is provided for phase lock loop synchronization. $\overline{\text{VFOE}}$ will go active when

a) Both HLT and HLD are True
b) Settling Time, if programmed, has expired
c) The 179X is inspecting data off the disk

If $\overline{\text{WF/VFOE}}$ is not used, leave open or tie to a 10K resistor to +5.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is

The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the FDC179X.



Head Load Timing

When both HLD and HLT are true, the FDC179X will then read from or write to the media. The "and" of HLD and HLT appears as a status bit in Type I status.

TYPE I COMMANDS FLAG SUMMARY
h = Head Load Flag (Bit 3)
h = 1, Load head at beginning h = 0, Unload head at beginning
V = Verify flag (Bit 2)
V = 1, Verify on destination track V = 0, No verify
r_1r_0 = Stepping motor rate (Bits 1-0)
Refer to Table 2 for rate summary
u = Update flag (Bit 4)
u = 1, Update Track register u = 0, No update

Type II Commands

The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the system must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled until true after a 15 msec delay. If the E flag is 0, HLD is made active and HLT is sampled with no delay until true. The ID field and Data Field format are shown below.

When an ID field is located on the disk, the FDC179X compares the Track Number on the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there is a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The FDC179X must find an ID field with a Track number, Sector number, side number, and CRC within four revolutions of the disk, otherwise, the Record not found status bit is set (Status bit 3) and the command is terminated with an interrupt.

Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The FDC179X will read or write multiple records starting with the sector presently in the sector register. The FDC179X will continue to read or write multiple records and update the sector register until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

If the Sector Register exceeds the number of sectors on the track, the Record-Not-Found status bit will be set.

The Type II commands also contain side select compare flags. When C = 0, no side comparison is made. When C = 1, the LSB of the side number is read off the ID Field of the disk and compared with the contents of the (S) flag. If the S flag compares with the side number recorded in the ID field, the 179X continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record-Not-Found status bit is set.

The FDC1795/7 READ SECTOR and WRITE SECTOR commands include a 'b' flag. The 'b' flag, in conjunction with the sector length byte of the ID Field, allows different byte lengths to be implemented in each sector. For IBM compatability, the 'b' flag should be set to a one. The 's' flag allows direct control over the SSO Line (Pin 25) and is set or reset at the beginning of the command, dependent upon the value of this flag.

Sector Length Table (1791/2/3/4 only)	
Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

Field Format

GAP III	ID AM	TRACK NUMBER	SIDE NUMBER	SECTOR NUMBER	SECTOR LENGTH	CRC 1	CRC 2	GAP II	DATA AM	DATA FIELD	CRC 1	CRC 2
ID FIELD										DATA FIELD		

In MFM only, IDAM and DATA AM are preceded by three bytes of A1 with clock transition between bits 4 and 5 missing

Read Sector

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the Record-Not-Found status bit is set and the operation is terminated.

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown below:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

Write Sector

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The FDC179X counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a_0 field of the command as shown below:

a_0	Data Address Mark (Bit 0)
1	Deleted Data Mark
0	Data Mark

The FDC179X then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in MFM. The WG output is then deactivated.

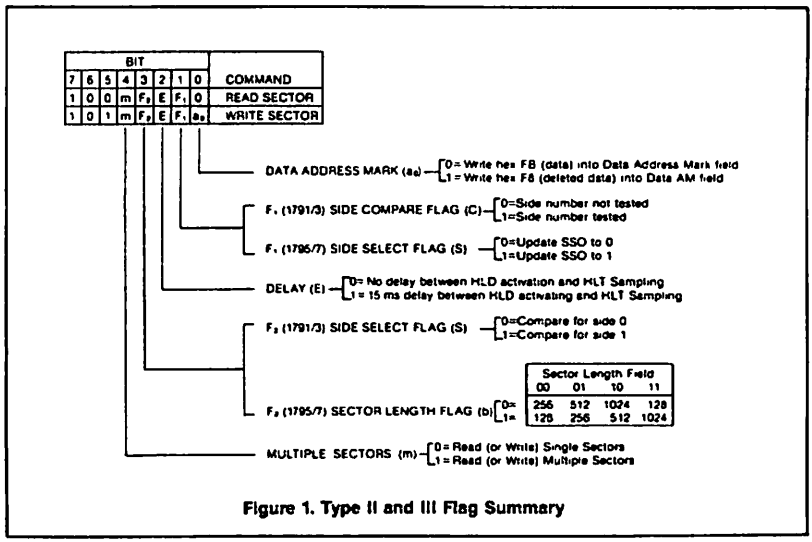


Figure 1. Type II and III Flag Summary

Type III Commands

There are three Type III Commands:

- READ ADDRESS—Read the next ID field (6 bytes) into the FDC.
- READ TRACK—Read all bytes of the entire track, including gaps.
- WRITE TRACK—Write all bytes to the entire track, including gaps.

Read Address

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the FDC179X checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register. At the end of the operation an interrupt is generated and the Busy Status is reset.

Read Track

Upon receipt of the Read Track command, the head is loaded and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. As each byte is assembled it is transferred to the Data Register and the Data Request is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. The accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated. RG is not activated during the Read Track Command. An internal side compare is not performed during a Read Track.

Write Track

Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which

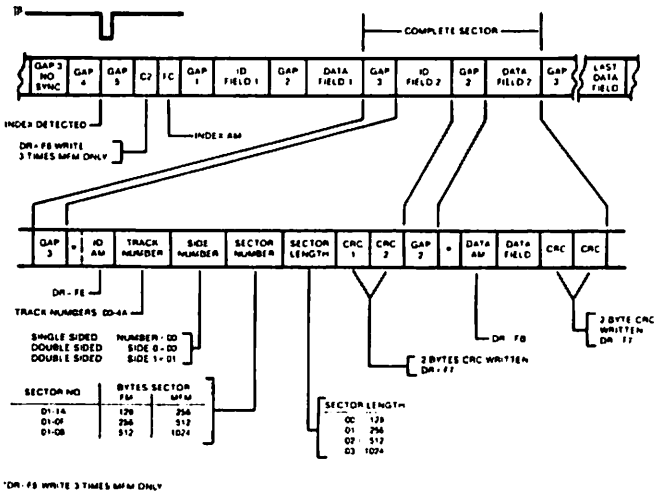


Figure 2. IBM Compatible Sector/Track Format

time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the interrupt is activated. If a byte is not present in the DR when needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream as shown in the table below. The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR in FM or by receipt of F5 in MFM.

Disk formatting (initialization) is accomplished by the Write Track command. Each byte for the entire track must be provided for proper formatting. This includes gap as well as data bytes.

The sequence required to format a diskette begins with positioning the Read/Write head at the desired track. Once this has been done, it is necessary to perform a Write Track command to store all the information on a track. The Write Track command uses DRQ to request each byte from the system MPU, starting with the byte at the beginning of the physical Index Pulse and ending with the last gap bytes at the end of the track. Figure 2 illustrates the IBM standard for track formatting.

Normally, each data byte stored on the diskette must be generated by the system MPU and passed into the FDC Data Register. However, there are exceptions to this rule. If a data byte of hex F5 through FE is entered into the Data Register, then the FDC recognizes this as an AM with missing clocks or CRC generation code. Consequently, F5 through FE must not be used in gaps, data fields, or ID fields, as this will disrupt normal operation of the FDC during formatting.

Type IV Commands

Force Interrupt is the only Type IV command. This command permits the MPU to terminate (abort) any command in progress. Figure 3 tabulates the Type IV command option bits.

The four bits, I_0-I_3, are used to select the condition of the interrupt occurrence. Regardless of which bit is set, any command currently being executed is immediately terminated and the Busy status bit is cleared, indicating "Not Busy". Then, when the condition is met, INTRQ goes high, causing the required interrupt.

If I_0-I_3 are all "0", no interrupt occurs, but any currently executing command is immediately terminated. If more than one condition is selected, then the interrupt occurs when any of the conditions is met.

To clear the interrupt, it is necessary to read the Status Register or to write the Command Register. An exception, however, is for I_3 = 1 (Immediate Interrupt). For this case, the interrupt is cleared with another Force Interrupt command with I_0-I_3 all low.

Status Register

The Status Register permits the MPU to monitor a variety of conditions in the FDC. For each command, the individual status bits have their own meaning. When a command is initiated (except for the Force Interrupt command), the Busy status bit is set and the others are cleared or updated. If the Force Interrupt command is entered when another command is in progress, the Busy status bit is cleared, but the others remain unaffected. However, if the Force Interrupt command is initiated when there is *not* another command in progress, the other status bits are cleared or updated and represent the Type I Command status. Figure 4 illustrates the meaning of the status bits for each command.

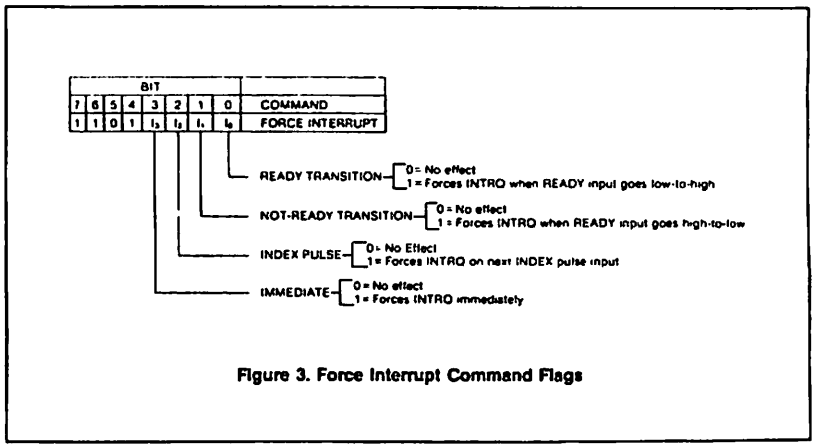


Figure 3. Force Interrupt Command Flags

Figure 4A. Status Register Summary

COMMAND	STATUS BIT							
	7	6	5	4	3	2	1	0
ALL TYPE I	Not Ready	Write Protect	Head Loaded	Seek Error	CRC Error	Track 0	Index	Busy
READ SECTOR	Not Ready	0	Record Type	Rec not Found	CRC Error	Lost Data	DRQ	Busy
WRITE SECTOR	Not Ready	Write Protect	Write Fault	Rec not Found	CRC Error	Lost Data	DRQ	Busy
READ ADDRESS	Not Ready	0	0	Rec not Found	CRC Error	Lost Data	DRQ	Busy
READ TRACK	Not Ready	0	0	0	0	Lost Data	DRQ	Busy
WRITE TRACK	Not Ready	Write Protect	Write Fault	0	0	Lost Data	DRQ	Busy

Figure 4B. Status Description for Type I Commands

BIT	NAME	MEANING
S7	NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6	PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{\text{WRPT}}$ input
S5	HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4	SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3	CRC ERROR	CRC encountered in ID field
S2	TRACK 00	When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{\text{TR00}}$ input.
S1	INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{\text{IP}}$ input.
S0	BUSY	When set command is in progress. When reset no command is in progress.

Figure 4C. Status Description for Type II and III Commands

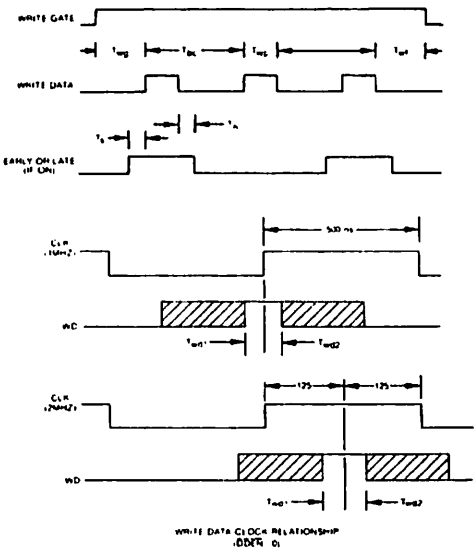
BIT	NAME	MEANING
S7	NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6	WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write. It indicates a Write Protect. This bit is reset when updated.
S5	RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the record-type code from data field address mark. 1=Deleted Data Mark. 0=Data Mark. On any Write. It indicates a Write Fault. This bit is reset when updated.
S4	RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3	CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2	LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1	DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0	BUSY	When set, command is under execution. When reset, no command is under execution.

Write Data Timing:

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
Write Data Pulse Width	T_{wp}	450	500	550	nsec	FM
		150	200	250	nsec	MFM
Write Gate to Write Data	T_{wg}		2		µsec	FM
			1		µsec	MFM
Write data cyle Time	T_{bc}		2, 3, or 4		µsec	± CLK Error
Early (Late) to Write Data	T_s	125			nsec	MFM
Early (Late) From Write Data	T_h	125			nsec	MFM
Write Gate off from WD	T_{wf}		2		µsec	FM
			1		µsec	MFM
WD Valid to Clk	T_{wd1}	100			nsec	CLK = 1 MHZ
		50			nsec	CLK = 2 MHZ
WD Valid after Clk	T_{wd2}	100			nsec	CLK = 1 MHZ
		30			nsec	CLK = 2 MHZ

These values are doubled when CLK - 1 MHz

Write Data Timing



MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +15V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}=+5V±5%, V_{DD}=+12V±5% unless otherwise noted)

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
DC CHARACTERISTICS							
Input Voltage Levels							
Low Level, V_{IL}					0.8	V	
High Level, V_{IH}			2.6			V	
Output Voltage Levels							
Low Level V_{OL}					0.45	V	I_{OL}=1.6 mA
High Level V_{OH}			2.8			V	I_{OH}=100 μA
Output Leakage, I_{LO}					10	μA	V_{OUT}=V_{DD}
Input Leakage, I_{IL}					10	μA	V_{IN}=V_{DD}
Output Capacitance				5		pf	
Input Capacitance				10		pf	
Power Dissipation					500	mW	
AC CHARACTERISTICS							
Processor Read Timing							
Address Setup Time		t_{SETR}	50			ns	Figure 5
Address Hold Time		t_{HLDR}	10			ns	Figure 5
RE Pulse Width (C_L=50pF)		t_{RE}	400			ns	Figure 5
DRQ Reset Time		t_{DRR}			500	ns	Figure 5
INTRQ Reset Time		t_{IRR}		500*	3000*	ns	Figure 5
Data Delay Time (C_L=50pF)		t_{DACC}			350	ns	Figure 5
Data Hold Time (C_L=50pF)		t_{DOH}	50		150	ns	Figure 5
Microprocessor Write Timing							
Address Setup Time		t_{SETW}	50			ns	Figure 6
Address Hold Time		t_{HLDW}	10			ns	Figure 6
WE Pulse Width		t_{WE}	350			ns	Figure 6
DRQ Reset Time		t_{DRR}			500	ns	Figure 6
INTRQ Reset Time		t_{IRR}		500*	3000*	ns	Figure 6
Data Setup Time		t_{DS}	250			ns	Figure 6
Data Hold Time		t_{DH}	70			ns	Figure 6
Disk Input Data Timing							
RAWREAD Pulse Width		t_{pw}	100*	200		ns	Figure 7, See Note
Clock Setup Time		t_{si}	40			ns	Figure 7 See Note
Clock Hold Time for MFM		t_{cd}	40			ns	Figure 7
Clock Hold Time for FM		t_{cb}	40			ns	Figure 7
RAWREAD Cycle Time		t_{bc}	1500			ns	1800 at 70°C, Figure 7
RCLK High Pulse Width	MFM	t_a	0.8	1*		μs	Figure 7
	FM		0.8	2*		μs	Figure 7
RCLK Low Pulse Width	MFM	t_b	0.8	1*		μs	Figure 7
	FM		0.8	2*		μs	Figure 7
RCLK Cycle Time	MFM	t_c		2*		μs	Figure 7
	FM			4*		μs	Figure 7
Miscellaneous Timing							
CLK Low Pulse Width		t_{CD1}	230	250	20000	ns	Figure 8
CLK High Pulse Width		t_{CD2}	200	250	20000	ns	Figure 8
STEP Pulse Width	MFM	t_{STP}		2*		μs	Figure 8
	FM			4*		μs	Figure 8
DIRC Setup Time		t_{DIR}		12		μs	Figure 8
MR Pulse Width		t_{MR}	50*			μs	Figure 8
IP Pulse Width		t_{IP}	10*			μs	Figure 8
WF Pulse Width		t_{WF}	10*			μs	Figure 8
CLK Cycle Time		t_{CYC}		0.5*		μs	Figure 8

*: These Values are doubled when CLK = 1 MHz.

Figure 5. Microprocessor Read Timing

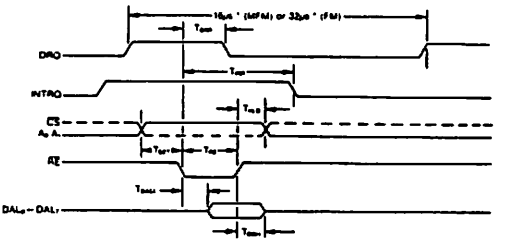


Figure 6. Microprocessor Write Timing

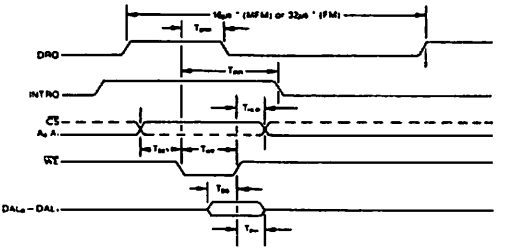


Figure 7. Disk Input Timing

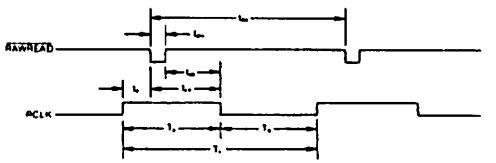
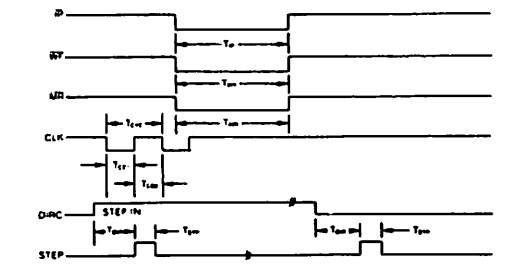


Figure 8. Miscellaneous Timing



DISK FORMATS

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

IBM 3740 Format

This single-density (FM) format utilizes 128 bytes/sector. The bytes to be generated by the system MPU for use in the execution of the Write Track command are shown in Figure 9.

IBM System 34 Format

This double-density (MFM) format utilizes 256 bytes/sector. The bytes to be generated by the system MPU for use in the execution of the Write Track command are shown in Figure 10.

Non-IBM Formats

Unique (non-IBM) formats are permissible providing the following restrictions are understood

- Sector length may only be 128, 256, 512, or 1024 bytes.
- Gap sizes must conform to Figure 11

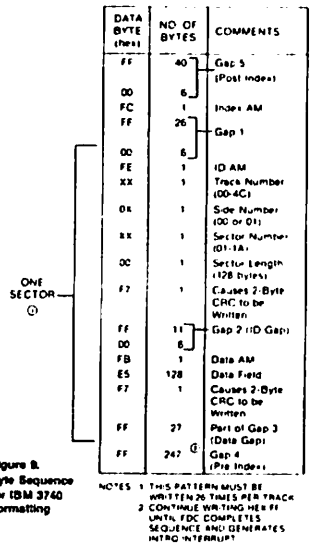


Figure 9. Byte Sequence for IBM 3740 Formatting

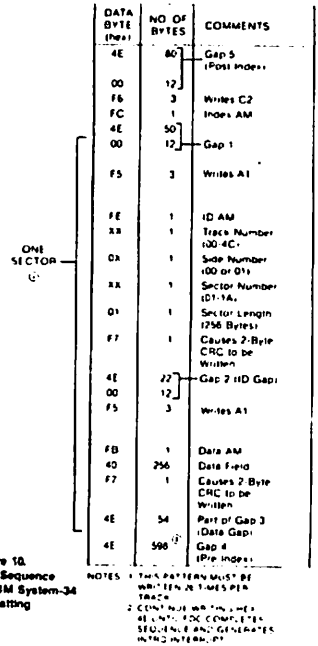


Figure 10. Byte Sequence for IBM System-34 Formatting

GAP	SINGLE DENSITY (FM)	DOUBLE DENSITY (MFM)	NOTE
Gap 1	16 bytes FF	16 bytes 4E	2
Gap 2	11 bytes FF 6 bytes 00	22 bytes 4F 12 bytes 00 3 bytes A1	1
Gap 3	10 bytes FF 4 bytes 00	16 bytes 4E 8 bytes 00 3 bytes A1	2
Gap 4	16 bytes FF	16 bytes 4E	2

NOTES 1 THESE BYTES COUNTS ARE EXACT
2 THESE BYTES COUNTS ARE MINIMUM EXCEPT FOR 3 BYTES A1 WHICH IS EXACT

Figure 11. Gap Size Limitations

STANDARD MICROSYSTEMS CORPORATION

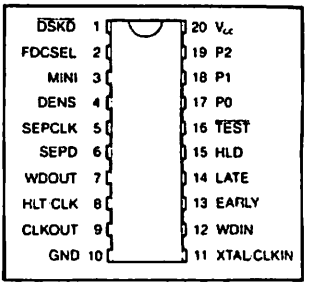
FDC 9229
FDC 9229B
FDC 9229T
FDC 9229BT

FLOPPY DISK INTERFACE CIRCUIT

FEATURES

- Digital Data Separator
  - Performs complete data separation function for floppy disk drives
  - Separates FM and MFM encoded data
  - No critical adjustments necessary
  - 5¼" and 8" compatible
- Variable Write Precompensation
- Internal Crystal Oscillator Circuit
- Track-Selectable Write Precompensation
- Retriggerable Head-Load Timer
- Compatible with the FDC 179X, 765, and other standard Floppy Disk Controllers
- COPLAMOS* n-channel MOS Technology
- Single +5 Volt Supply
- TTL Compatible

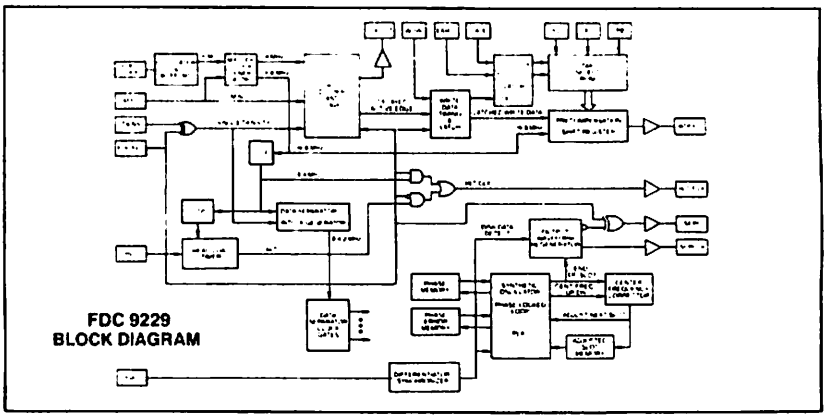
PIN CONFIGURATION



FUNCTIONAL DESCRIPTION

The FDC 9229 B is an MOS integrated circuit designed to complement either the 179X or 765 (8272) type of floppy disk controller chip. It incorporates a digital data separator, write precompensation logic, and a head-load timer in one 0.3-inch wide 20-pin package. A single pin will configure the chip to work with either the 179X or 765 type of controller. The FDC 9229 B provides a number of different dynamically selected precompensation values so that different values may be used when writing to the inner and outer tracks of the floppy disk drive. The FDC 9229 B operates from a +5V supply and simply requires that a 16 or 8 MHz crystal or TTL-level clock be connected to the XTAL/CLKIN pin. All inputs and outputs are TTL compatible.

The FDC 9229 is available in four versions: The FDC 9229/T are intended for 5¼" disks and the FDC 9229B/T for 5¼" and 8" disks. The FDC 9229 B have an internal crystal oscillator circuit; the FDC 9229T/BT require an external clock.



FDC 9229
BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	I/O	DESCRIPTION
1	$\overline{DSKD}$	I	This input is the raw read data received from the drive. (This input is active low.)
2	FDCSEL	I	This input signal, when low, programs the FDC 9229/B for a 179X type of LSI controller. When FDCSEL is high, the FDC 9229/B is programmed for a 765 (8272) type of controller. (See fig. 4.)
3	MINI	I	The state of this input determines whether the FDC 9229/B is configured to support 8" or 5¼" floppy disk drive interfaces. It is used in conjunction with the DENS input to prescale the clock for the data separator. The state of this input also alters the CLKOUT frequency, the precompensation value, the head load delay time (when in 179X mode) and the HLT/CLK frequency (when in 765 mode). (See figs. 2, 3, and 4.)
4	DENS	I	The state of this input determines whether the FDC 9229/B is configured to support single density (FM) or double density (MFM) floppy disk drive interfaces. It is used in conjunction with the MINI input to prescale the clock for the data separator. The state of this input also alters the CLKOUT frequency when in the 765 mode. (See figs. 2, 3, and 4.)
5	SEPCLK	O	A square-wave window clock signal output derived from the $\overline{DSKD}$ input.
6	SEPD	O	This output is the regenerated data pulse derived from the raw data input ($\overline{DSKD}$). This signal may be either active low or active high as determined by FDCSEL (pin 2).
7	WDOUT	O	The precompensated WRITE DATA stream to the drive.
8	HLT/CLK	O	When in the 765 mode (FDCSEL high), this output is the master clock to the floppy disk controller. When in the 179X mode, this signal goes high after the head load delay has occured following the HLD input going high. This output is retriggerable. (See fig. 3.)
9	CLKOUT	O	This signal is the write clock to the floppy disk controller. Its frequency is determined by the state of the MINI, DENS, and FDCSEL input pins. (See fig. 3.)
10	GND		Ground
11	XTAL/CLKIN	I	This input is for direct connection to a 16 MHz or 8 MHz crystal (FDC 9229/B only). The other pin of the crystal is grounded. XTAL/CLKIN may alternatively be connected to a single-phase TTL-level clock. The FDC 9229T and BT require an external TTL-level clock.
12	WDIN	I	The write data stream from the floppy disk controller.
13	EARLY	I	When this input is high, the current WRITE DATA pulse will be written early to the disk.
14	LATE	I	When this input is high, the current WRITE DATA pulse will be written late to the disk. When both EARLY and LATE are low, the current WRITE DATA pulse will be written at the nominal position.
15	HLD	I	This input is only used in 179X mode. A high level at this input causes a high level on the HLT/CLK output after the specified head-load time delay has elapsed. The delay is selected by the state of the MINI output. (See fig. 3.)
16	$\overline{TEST}$	I	This input (when low) decreases the head-load time delay and initializes the data separator. This pin is for test purposes only. This input has an internal pull-up resistor and should be tied high or disconnected for normal operation.
17	P0	I	P2-P0 select the amount of precompensation applied to the write data. (See fig. 2.)
18	P1	I	
19	P2	I	
20	V_{CC}		+5 VOLT SUPPLY

OPERATION

Data Separator

The XTAL/CLKIN input clock is internally divided by the FDC 9229'B to provide an internal clock. The division ratio is selected by the FDCSEL, MINI and DENS inputs depending on the type of drive used. (See fig. 1.)

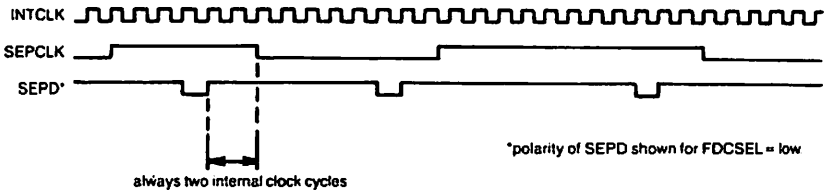
The FDC 9229/B detects the leading (negative) edges of the disk data pulses and adjusts the phase of the internal clock to provide the SEPCLK output.

Separate short- and long-term timing correctors assure accurate clock separation.

The SEPCLK frequency is nominally 1/16 the internal clock frequency. Depending on the internal timing correction, the duration of any SEPCLK half-cycle may vary from a nominal of 8 to a minimum of 6 and a maximum of 11 internal clock cycles.

INPUTS			DIVISOR
FDCSEL	DENS	MINI	f(XTAL/CLKIN)/f(INTCLK)
0	0	0	2
0	0	1	4
0	1	0	4
0	1	1	8
1	0	0	4
1	0	1	8
1	1	0	2
1	1	1	4

FIG. 1



Precompensation

The desired precompensation delay is determined by the state of the P0, P1 and P2 inputs of the FDC 9229'B as per fig. 2. Logic levels present on these pins may be changed dynamically as long as the inputs are stable during the time the floppy disk controller is writing to the drive and the inputs meet the minimum setup time with respect to the write data from the floppy disk controller.

MINI	P2	P1	P0	PRECOMP VALUE
0	0	0	0	0 ns
0	0	0	1	62.5 ns
0	0	1	0	125 ns
0	0	1	1	187.5 ns
0	1	0	0	250 ns
0	1	0	1	250 ns
0	1	1	0	312.5 ns
0	1	1	1	312.5 ns
1	0	0	0	0 ns
1	0	0	1	125 ns
1	0	1	0	250 ns
1	0	1	1	375 ns
1	1	0	0	500 ns
1	1	0	1	500 ns
1	1	1	0	625 ns
1	1	1	1	625 ns

NOTE: All values shown are obtained with a 16 MHz reference clock. Multiply pre-comp values by two for 8 MHz operation.

FIG. 2 WRITE PRECOMPENSATION VALUE SELECTION

Head Load Timer

The head load time delay is either 40 ms or 80 ms, depending on the state of MINI. (See fig. 3.) The purpose of this delay is to ensure that the head has enough time to engage properly. The head load timer is only used in the 179X mode; it is non-functional in the 765 mode.

The FDC 179X initiates the loading of the floppy disk drive head by setting HLD high. The controller then waits the programmed amount of time until the HLT signal from the FDC 9229 B goes high before starting a read or write operation.

INPUTS			OUTPUTS	
FDCSEL	DENS	MINI	CLKOUT	HLT CLK
0	0	0	2 MHz	40 ms*
0	0	1	1 MHz	80 ms*
0	1	0	2 MHz	40 ms*
0	1	1	1 MHz	80 ms*
1	0	0	500 KHz	8 MHz
1	0	1	250 KHz	4 MHz
1	1	0	1 MHz	8 MHz
1	1	1	500 KHz	4 MHz

NOTE: All values shown are obtained with a 16 MHz reference clock. Divide all frequencies and multiply all periods by two for 8 MHz operation.

*May be mask programmed at factory to any value from 1 to 512 ms in 15.625 µs increments (MINI low) or 1 to 1024 ms in 31.25 µs increments (MINI high).

FIG. 3 CLOCK AND HEAD LOAD TIME DELAY SELECTION

INPUTS			FLOPPY DISK	FLOPPY DISK	FLOPPY DISK
FDCSEL	DENS	MINI	DRIVE TYPE	DRIVE DENSITY	CONTROLLER TYPE
0	0	0	8" DRIVE	DOUBLE	179X
0	0	1	5¼" DRIVE	DOUBLE	179X
0	1	0	8" DRIVE	SINGLE	179X
0	1	1	5¼" DRIVE	SINGLE	179X
1	0	0	8" DRIVE	SINGLE	765 (8272)
1	0	1	5¼" DRIVE	SINGLE	765 (8272)
1	1	0	8" DRIVE	DOUBLE	765 (8272)
1	1	1	5¼" DRIVE	DOUBLE	765 (8272)

FIG. 4 FLOPPY DISK DRIVE AND CONTROLLER SELECTION

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	− 55° to + 150°C
Lead Temperature (soldering, 10 sec.)	+ 300°C
Positive Voltage on any I/O Pin, with respect to ground	+ 8.0V
Negative Voltage on any I/O Pin, with respect to ground	− 0.3V
Power Dissipation	0.75W

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
DC CHARACTERISTICS					
INPUT VOLTAGE					
Low Level V_{IL}	-0.3		0.8	V	Except XTAL/CLKIN
High Level V_{IH}	2.0		(V_{CC})	V	
XTAL CLKIN INPUT VOLTAGE					
AC Amplitude	1.0			V_{p-p}	XTAL/CLKIN only; input is AC-coupled
Instantaneous voltage	-0.3		(V_{CC})	V	
OUTPUT VOLTAGE					
Low Level V_{OL}			0.4	V	I_{OL} = 1.6 mA except HLT/CLK
					I_{OL} = 0.4 mA, HLT/CLK only
High Level V_{OH}	2.4			V	I_{OH} = − 100 µA except HLT/CLK
					I_{OH} = − 400 µA, HLT/CLK only
POWER SUPPLY CURRENT					
I_{CC}			100	mA	
INPUT LEAKAGE CURRENT					
I_{LI}			±10	µA	V_{IN} = 0 to V_{CC}
INPUT CAPACITANCE			10	pF	Except CLKIN
C_{IN}			25	pF	CLKIN only

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
AC ELECTRICAL CHARACTERISTICS	(All times assume XTAL/CLKIN = 16 MHz unless otherwise specified)				
XTAL CLKIN frequency	3.95	16	16.2	MHz	FDC 9229B
	3.95	8	8.1	MHz	FDC 9229
XTAL CLKIN DUTY CYCLE	25		75	%	
t_{WL}	465	500	515	ns	FDCSEL = low; MINI = high
	215	250	265	ns	FDCSEL = low; MINI = low
	90	125	140	ns	FDCSEL = high.
t_{WH}	280	312.5	350	ns	
t_{RI}	50		400	ns	
t_{WRC}	0		400	ns	
t_{WP}		562.5		ns	
t_{DS}		precomp value			See fig. 2.
t_{DH}		2 x precomp value			See fig. 2.
t_{IR}	1.0			µs	

CRYSTAL SPECIFICATIONS

Frequency (8" Disk Drive) 16 MHz, at Cut
(5¼" Disk Drive) 8 MHz, at Cut
Holder Preferred: HC - 18 V
Frequency and stability tolerance: ± .05% from 0°C to 70°C
Series Resistance: 50 ohm max

AC TIMING CHARACTERISTICS