Ordering number : ENN*6830

CMOS IC

LC680100A

32-Bit RISC Microcontroller

Preliminary

Overview

The LC680100A is a 32 bit microcontroller developed exclusively by Sanyo, based on a 32 bit RISC CPU and incorporating on a single chip a high speed multiplier, 2kB of cache RAM, 2kB data RAM, DRAM control unit, external memory control unit and peripheral

It is an ideal control device for digital cameras, color printers and hand held data terminals.

Features

(1) CPU core	:32 bit RISC (Speed: 15MHz, Instruction cycle time: 67ns)
(2) High Speed Multiplier	:16bit x 16bit (in 1 instruction cycle)
(3) Instruction cache RAM	:2kB (512x32bit)
(4) Data RAM	:2kB (512x32bit)
(5) DRAM Control Unit	
(6) External memory bus control unit	
(7) I/O port	:One 16 bit I/O port, one 8 bit I/O port
(8) UART	:Two full duplex asynchronous channels (one channel has 16bit FIFO)
(9) Serial I/O	:One three-wire synchronous clock, 8 bit
(10) Timer	:4 channels (TM0 = 16bit + 16bit) (TM1, TM2, TM3 = 8bit + 8bit)
(11) PWM Output	:Three 8 bit resolution outputs (Common with TM1, TM2, TM3)
(12) Interrupt controller	:13 source events (5 internal, 8 external), 5 vectored
(13) OSC circuit	:Two types: main and RC. VCO/PLL is built-in, frequency multiplication possible.
(14) Standby	:Standby (HOLD) and sleep (HALT) modes available
(15) VDD	:3.3V typ.

Package and Pins

SQFP100, 100 pins

Development tools

A C compiler, assembler and emulator are available to be run on a PC.

SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

System Block Diagram

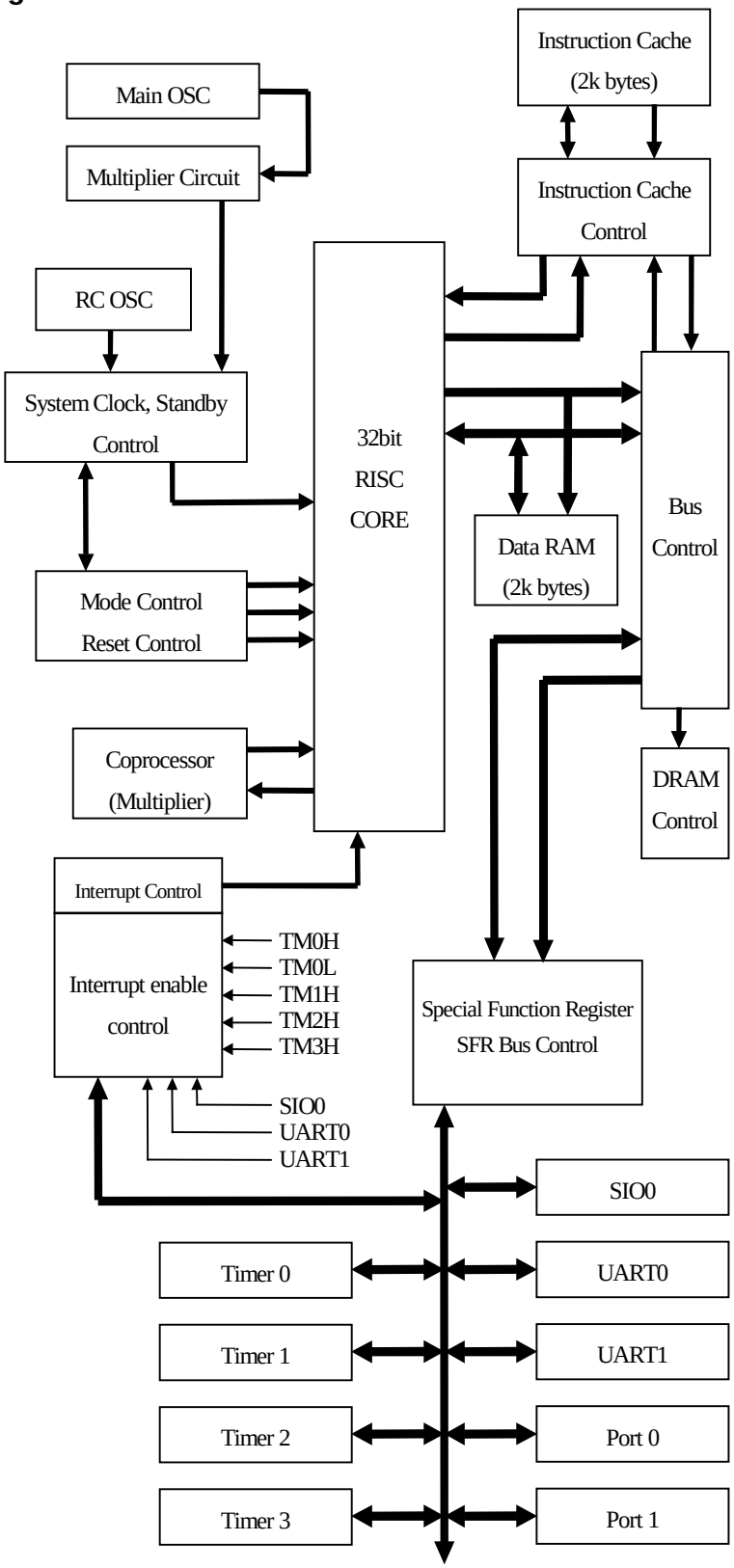
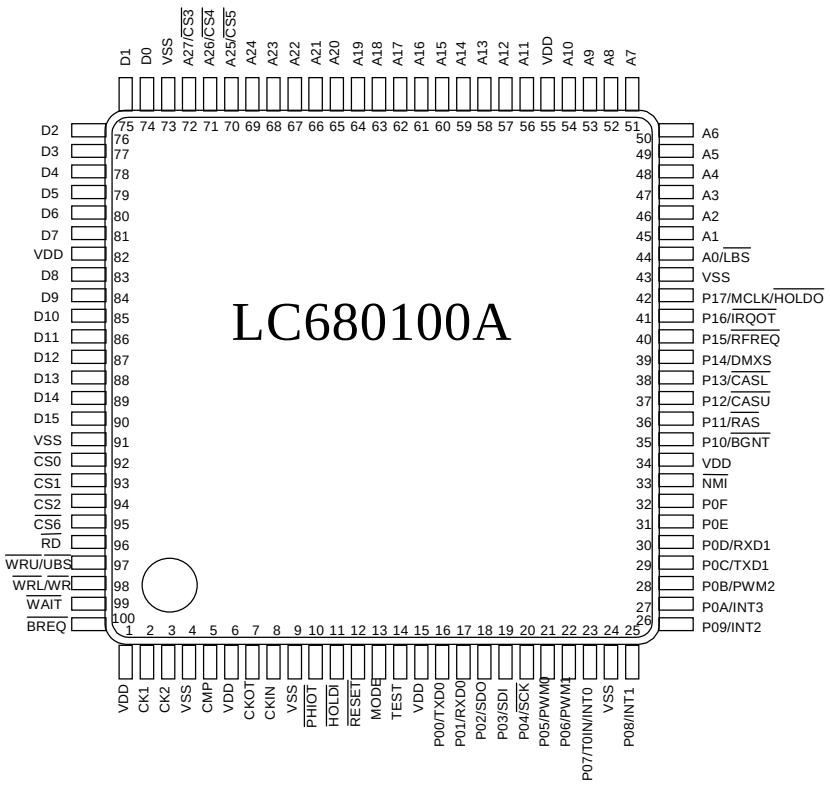


Figure 1 LC680100A System Block Diagram

Terminal Assignment Diagram

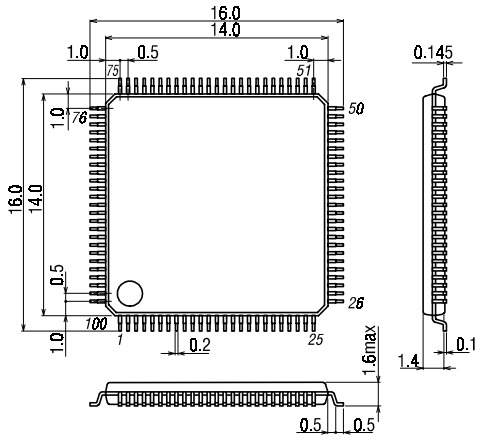
(SQFP100, 0.5mm pitch)



Package Dimension

(unit : mm)

3181B



SANYO : SQFP-100

Terminal Functions

Note: PU = pull-up

Pin Number	Pin Name	I/O	Function Description	Pin Format
1,6,15,34,55,82	VDD	-	Power supply +ve	-
4,9,24,43,73,91	VSS	-	Power supply -ve	-
2	CK1	I	Input to main oscillator	Schmitt Input
3	CK2	O	Output from main oscillator	CMOS output
5	CMP	I/O	Phase comparator filter pin (multiplier circuit).	Schmitt Input•Tristate output
7	CKOT	O	CK1 or half frequency clock output from multiplier	CMOS output
8	CKIN	I	External clock input	Schmitt Input
10	$\overline{\text{PHIOT}}$	O	System clock output	CMOS output
11	$\overline{\text{HOLDI}}$	I	HOLD request input	Schmitt Input
12	$\overline{\text{RESET}}$	I	Reset terminal	Schmitt Input
13	MODE	I	Bus mode setting at reset	Schmitt Input
14	TEST	I	Test input (Normally connected to VSS)	Schmitt Input
16	P00/TXD0	I/O	PORT0 bit0 I/O. Also UART0 send	•Used as input: Schmitt Input; presence of PU resistor software selectable. •Used as Output: CMOS/N-ch OD mode software selectable.
17	P01/RXD0	I/O	PORT0 bit1 I/O. Also UART0 receive	
18	P02/SDO	I/O	PORT0 bit2 I/O. Also SIO0 data out	
19	P03/SDI	I/O	PORT0 bit3 I/O. Also SIO0 data in	
20	P04/$\overline{\text{SCK}}$	I/O	PORT0 bit4 I/O. Also SIO0 clock	
21	P05/PWM0	I/O	PORT0 bit5 I/O. Also PWM0 output	
22	P06/PWM1	I/O	PORT0 bit6 I/O. Also PWM1 output	
23	P07/T0IN/INT0	I/O	PORT0 bit7 I/O. Timer0 event input INT0 input	
25	P08/INT1	I/O	PORT0 bit8 I/O. INT1 input	
26	P09/INT2	I/O	PORT0 bit9 I/O. INT2 input	
27	P0A/INT3	I/O	PORT0 bit10 I/O. INT3 input	
28	P0B/PWM2	I/O	PORT0 bit11 I/O. PWM2 output	
29	P0C/TXD1	I/O	PORT0 bit12 I/O. UART1 send	
30	P0D/RXD1	I/O	PORT0 bit13 I/O. UART1 receive	
31	P0E	I/O	PORT0 bit14 I/O.	
32	P0F	I/O	PORT0 bit15 I/O.	

Pin Number	Pin Name	I/O	Function Description	Pin Format
33	$\overline{\text{NMI}}$	I	NMI interrupt	Schmitt Input
35	P10/$\overline{\text{BGNT}}$	I/O	PORT1 bit0 input. Also bus grant output.	Schmitt Input•Tristate output
36	P11/$\overline{\text{RAS}}$	I/O	PORT1 bit1 input. Also DRAM control RAS signal out.	
37	P12/$\overline{\text{CASU}}$	I/O	PORT1 bit2 input. Also DRAM control CASU signal out.	
38	P13/$\overline{\text{CASL}}$	I/O	PORT1 bit3 input. Also DRAM control CASL signal out.	
39	P14/$\overline{\text{DMXS}}$	I/O	PORT1 bit4 input. Also DRAM control DMXS signal out.	
40	P15/$\overline{\text{RFREQ}}$	I/O	PORT1 bit5 input. Also DRAM control RFREQ I/O.	Schmitt Input•PU Output
41	P16/$\overline{\text{IRQOT}}$	I/O	PORT1 bit6 input. Also IRQOT output.	Schmitt Input•Tristate output
42	P17/MCLK/$\overline{\text{HOLD0}}$	I/O	PORT1 bit7 input. MCLK output, HOLD state output	
44	A0/$\overline{\text{LBS}}$	I/O	Bus Address bit0 or Lower byte strobe signal.	Schmitt Input•Tristate output
45 to 54, 56 to 69	A1to A24	I/O	Bus Address bit1 to 24.	
70	A25/$\overline{\text{CS5}}$	I/O	Bus Address bit25 or CS5.	
71	A26/$\overline{\text{CS4}}$	I/O	Bus Address bit26 or CS4	
72	A27/$\overline{\text{CS3}}$	I/O	Bus Address bit27 or CS3.	
74 to 81, 83 to 90	D0 to D15	I/O	Bus data bit0 to 15	Schmitt Input•Tristate output
92	$\overline{\text{CS0}}$	I/O	$\overline{\text{CS0}}$	Schmitt Input•Tristate output
93	$\overline{\text{CS1}}$	I/O	$\overline{\text{CS1}}$	
94	$\overline{\text{CS2}}$	I/O	$\overline{\text{CS2}}$	
95	$\overline{\text{CS6}}$	I/O	$\overline{\text{CS6}}$	
96	$\overline{\text{RD}}$	I/O	Bus read signal.	Schmitt Input•Tristate output
97	$\overline{\text{WRU}}$/$\overline{\text{UBS}}$	I/O	Upper byte write signal or Upper byte strobe.	
98	$\overline{\text{WRL}}$/$\overline{\text{WR}}$	I/O	Upper byte write signal or Write.	
99	$\overline{\text{WAIT}}$	I/O	Bus cycle wait	Schmitt Input•PU output
100	$\overline{\text{BREQ}}$	I	Bus request.	Schmitt Input

1. Absolute Maximum Ratings at Ta = 25°C, VSS = 0V

Parameter	Symbol	Pins	Conditions	Ratings	Unit
Supply voltage	VDDmax	VDD Note1		-0.3 to +4.6	V
Input voltage	VI(1)	Pins for each input only		-0.3 to VDD+0.3	V
Output voltage	VO(1)	Pins for each output only		-0.3 to VDD+0.3	V
Input/Output voltage	VIO(1)	Pins for both input and output		-0.3 to VDD+0.3	V
High level peak output current	IOPH(1)	Each output pin	Current at each pin	-5	mA
High level total output current	∑IOAH(1)	P00 to P08	Total of 9 pins	-80	mA
	∑IOAH(2)	P09 to P0F	Total of 7 pins	-80	mA
Low level peak output current	IOPL(1)	Each output pin	Current at each pin	20	mA
Low level total output current	∑IOAL(1)	P00 to P07	Total of 8 pins	80	mA
	∑IOAL(2)	P08 to P0F	Total of 8 pins	80	mA
Maximum power consumption	Pdmax	SQFP100 Note2	Ta = -20 to 70°C	440	mW
Operating temperature range	Topg			-20 to +70	°C
Storage temperature range	Tstg			-55 to +125	°C

Note1:All VDD terminals (pin1, 6, 15, 34, 55, 82) should be connected externally.
All VSS terminals (pin4, 9, 24, 43, 73, 91) should be connected externally.
Note2:Reflow method is recommended when soldering the SQFP package.

2. Recommended Operating Range at Ta = -20 to 70°C, VSS = 0V

Parameter	Symbol	Pins	Conditions	Ratings			Unit
				Min.	Typ.	Max.	
Operating supply voltage range	VDD (1)	VDD		3.0	3.3	3.6	V
Supply voltage (Memory hold)	VHD	VDD	Keep RAM and Register data in Standby mode.	2.5		3.6	V
High level input voltage	VIH(1)	Input pins except CK1		0.7VDD		VDD	V
	VIH(2)	CK1		0.7VDD		VDD	
Low level input voltage	VIL(1)	Input pins except CK1		VSS		0.3VDD	V
	VIL(2)	CK1		VSS		0.3VDD	
Operation cycle time	tCYC(1)	CKIN	300K to 15MHz	66		3333	ns
	tCYC(2)	CK1	400K to 15MHz (VCO is not used.)	132		5000	
External system clock frequency	fEXCKIN	CKIN	Figure 1	300k		15M	Hz
	fEXCK1	CK1	Figure 1	400k		15M	
External clock pulse width	tCKINL tCKINH	CKIN	Figure 1	28			ns
	tCK1L tCK1H	CK1	Figure 1	28			
External clock rising and falling time	tEXR tEXF	CKIN, CK1	Figure 1			5	ns
Operation frequency range	fCK1	CK1, CK2	Figure 2, Table 1	400k		8M	Hz

3. Electrical Characteristics at Ta = -20 to 70°C, VSS = 0V, VDD = 3.0 to 3.6V

Parameter	Symbol	Pins	Conditions	Ratings			Unit
				Min.	Typ.	Max.	
High level input current	IIH(1)	Pins for each input only	VIN = VDD			5	μA
	IIH(2)	Pins for both input and output	VIN = VDD Output disabled			5	
Low level input current	IIL(1)	Pins for each input only	VIN = VSS	-5			μA
	IIL(2)	P15/$\overline{\text{RFREQ}}$,$\overline{\text{WAIT}}$	VIN = VSS Output disabled	-5			
	IIL(3)	Input/output commonly terminals except written above	VIN = VSS Output disabled	-5			
High level output voltage	VOH(1)	Port0 with PU option, P15/$\overline{\text{RFREQ}}$	IOH = -0.05mA	VDD-0.5			V
	VOH(2)	Input/output commonly terminals except written above, CKOT, $\overline{\text{PHIOT}}$	IOH = -1mA	VDD-0.5			
Low level output voltage	VOL(1)	Pins for each output only	IOL = 4mA			0.4	V
	VOL(2)	Pins for both input and output	IOL = 4mA			0.4	
PU resistor	rPU	Port0 with PU option, P15/$\overline{\text{RFREQ}}$		1K		20K	Ω
Hysterisis voltage	vHIS	Each input only, I/O terminal			0.1		VDD
External interrupt pulse width	tINTL	$\overline{\text{NMI}}$	Figure 4	2			Tcyc
	tINTH	INT0 to INT3		4			
Reset input pulse width	tRESL	$\overline{\text{RESET}}$	Figure 4	2			ms
VCO frequency	fVCO	CKOT	Figure 5	4M		16M	Hz
VCO lock-up time	tLOCK	CMP,CKOT	Figure 5, cCMP = 0.1μF		10		ms
RC oscillation frequency	fRC	Built-in RC oscillation circuit		300k		1M	Hz
Ceramic oscillation stabilizing time	tCF	CK1,CK2	Figure 3			10	ms
Current consumption in run mode	IDDRUN	VDD	CKIN=15MHz		60	120	mA
Current consumption in sleep mode	IDDSLP	VDD			50	100	mA
Current consumption in standby mode	IDDSTY	VDD			10	200	μA
Pin capacitance	cP	All pins			10		PF

4. Serial Input/Output Characteristics at Ta = -20 to 70°C, VSS = 0V, VDD = 3.0 to 3.6V, with the load in Figure 14

Parameter	Symbol	Pins	Conditions	Ratings			Unit
				Min.	Typ.	Max.	
Input clock cycle time	tSCK	$\overline{SCK}$ input	Figure 6	16			Tcyc
Input clock L pulse width	tSCKL	$\overline{SCK}$ input	Figure 6	533			ns
Input clock H pulse width	tSCKH	$\overline{SCK}$ input	Figure 6	533			ns
Output clock cycle time	tSCKO	$\overline{SCK}$ output	Figure 6	16			Tcyc
Output clock L pulse width	tSCKOL	$\overline{SCK}$ output	Figure 6	8			Tcyc
Output clock H pulse width	tSCKOH	$\overline{SCK}$ output	Figure 6	8			Tcyc
Input data set up time	tsDI	$\overline{SCK}$, SDI	Figure 6	200			ns
Input data hold time	thDI	$\overline{SCK}$, SDI	Figure 6	50			ns
Output delay time	tdDO	$\overline{SCK}$, SDO	Figure 6		100	130	ns

5. Bus Timing at Ta = -20 to 70°C, VSS = 0V, VDD = 3.0 to 3.6V, with the load in Figure14

Parameter	Symbol	Pins	Conditions	Ratings			Unit
				Min.	Typ.	Max.	
Address output delay time	tAAD	A27 to A0	Figure 7, Figure 8			75	ns
Address output hold time	tADA	A27 to A0	Figure 7, Figure 8			75	
CS delay time (1)	tACS	$\overline{CSn}$	Figure 7, Figure 8			45	
CS hold time (1)	tCSA	$\overline{CSn}$	Figure 7, Figure 8			55	
RD delay time (1)	tARD	$\overline{RD}$	Figure 7			45	ns
RD hold time (1)	tRDA	$\overline{RD}$	Figure 7			55	
Read data set up time (1)	tsRD1	D15 to D0	Figure 7	30			
Read data hold time (1)	thRD1	D15 to D0,	Figure 7	0			
WR delay time (1)	tAWR	$\overline{WRU}$, $\overline{WRL}$	Figure 8			45	ns
WR hold time (1)	tWRA	$\overline{WRU}$, $\overline{WRL}$	Figure 8			55	
Write data delay time (1)	tdWD1	D15 to D0, $\overline{WRU}$, $\overline{WRL}$	Figure 8			70	
Write data hold time (1)	thWD1	D15 to D0, $\overline{WRU}$, $\overline{WRL}$	Figure 8	0		30	
Bus request input setup time	tsBRQ	CKIN, $\overline{BREQ}$	Figure 12	30			ns
Bus request input hold time	thBRQ	CKIN, $\overline{BREQ}$	Figure 12	30			
BGNT output delay time	tdBGT	CKIN, $\overline{BGNT}$	Figure 12			50	
Bus release delay time	tdBOF	CKIN, A27 to A0, $\overline{RD}$,$\overline{WRU}$,$\overline{WRL}$	Figure 12			50	
WAIT set up time	tsWAIT	CKIN, $\overline{WAIT}$		30			
WAIT input hold time	thWAIT	CKIN, $\overline{WAIT}$		30			

6. DRAM Timing at Ta = -20 to 70°C, VSS = 0V, VDD = 3.0 to 3.6V, with the load in Figure 14

Parameter	Symbol	Pins	Conditions	Ratings			Unit
				Min.	Typ.	Max.	
Address (ROW) delay time	tAROW	A27 to A0	Figure 9, Figure 10			75	ns
Address (COL) delay time	tACOL	A27 to A0	Figure 9, Figure 10			55	
Address (COL) hold time	tCOLA	A27 to A0	Figure 9, Figure 10			70	
RAS delay time	tARAS	$\overline{RAS}$	Figure 9, Figure 10			65	
RAS hold time	tRASA	$\overline{RAS}$	Figure 9, Figure 10			50	
DMXS delay time	tDMXSR	DMXS	Figure 9, Figure 10			70	
DMXS hold time	tDMXSC	DMXS	Figure 9, Figure 10			50	
CASL•CASU delay time	tACAS(L/U)	$\overline{CASU}$, $\overline{CASL}$	Figure 9, Figure 10			65	
CASL•CASU hold time	tCAS(L/U)A	$\overline{CASU}$, $\overline{CASL}$	Figure 9, Figure 10			50	
Read data set up time (2)	tsRD2	D15 to D0	Figure 9	30			ns
Read data hold time (2)	thRD2	D15 to D0, $\overline{RD}$	Figure 9	0			
WRL•WRU delay time	tAWR(L/U)	$\overline{WRU}$, $\overline{WRL}$	Figure 10			45	ns
WRL•WRU hold time	tWR(L/U)A	$\overline{WRU}$, $\overline{WRL}$	Figure 10			50	
Write data delay time (2)	tdWD2	D15 to D0, $\overline{WRU}$, $\overline{WRL}$	Figure 10			70	
Write data hold time (2)	thWD2	D15 to D0, $\overline{WRU}$, $\overline{WRL}$	Figure 10	0			

Table 1. Guaranteed Value for the Ceramic Oscillators

Oscillator	Manufacturer	Oscillator	C1	C2
4MHZ (External Capacitor)	Murata	CSA4. OOMG	33pF	33pF
4MHZ (Capacitor built-in)		CST4. OOMGW	(30pF)	(30pF)
8MHZ (External Capacitor)		CSA8. OOMTZ	33pF	33pF
8MHZ (Capacitor built-in)		CST8. OOMTW	(30pF)	(30pF)

Figure1 External Clock Input

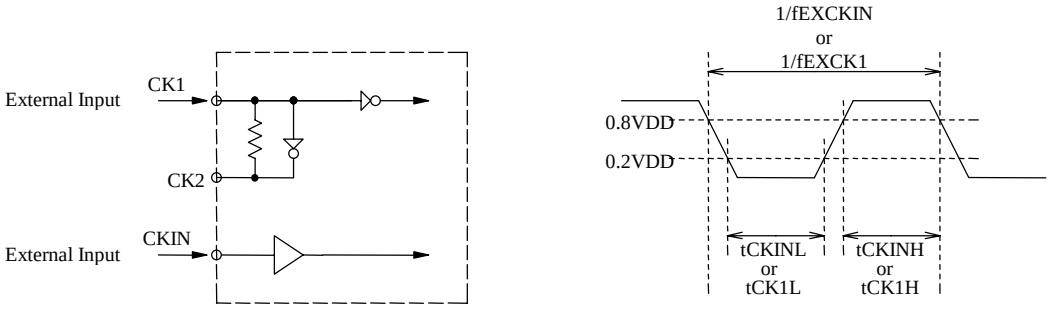


Figure2 Ceramic Oscillation

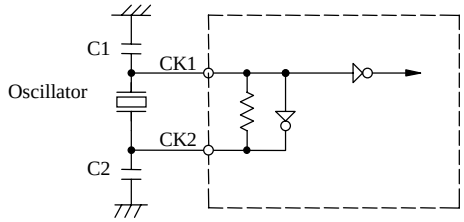


Figure3 Oscillation Stabilizing Time

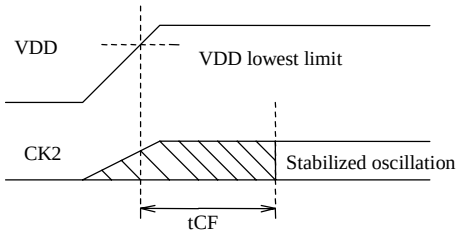


Figure4 External Pulse Input

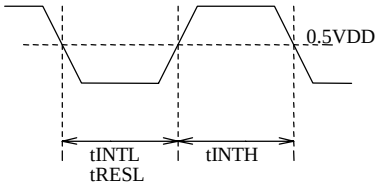


Figure5 VCO

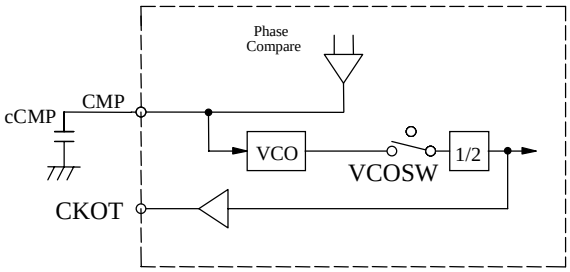


Figure6 Serial Input/Output Timing

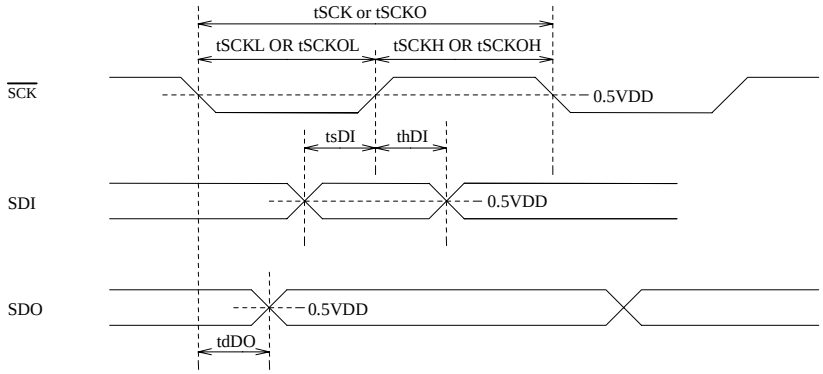


Figure7 External Bus Read Timing

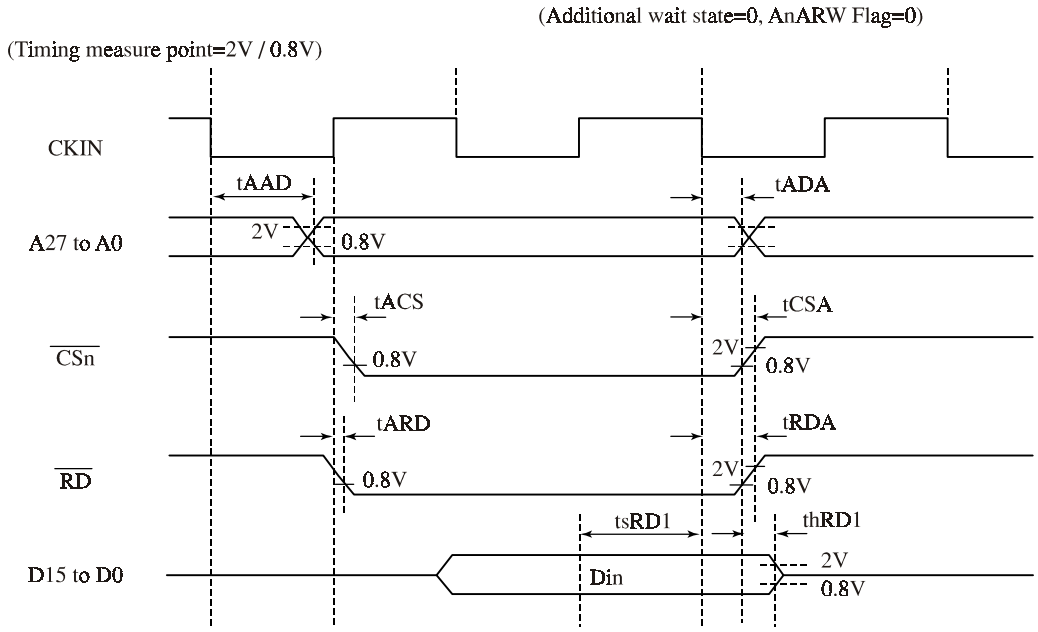


Figure8 External Bus Write Timing

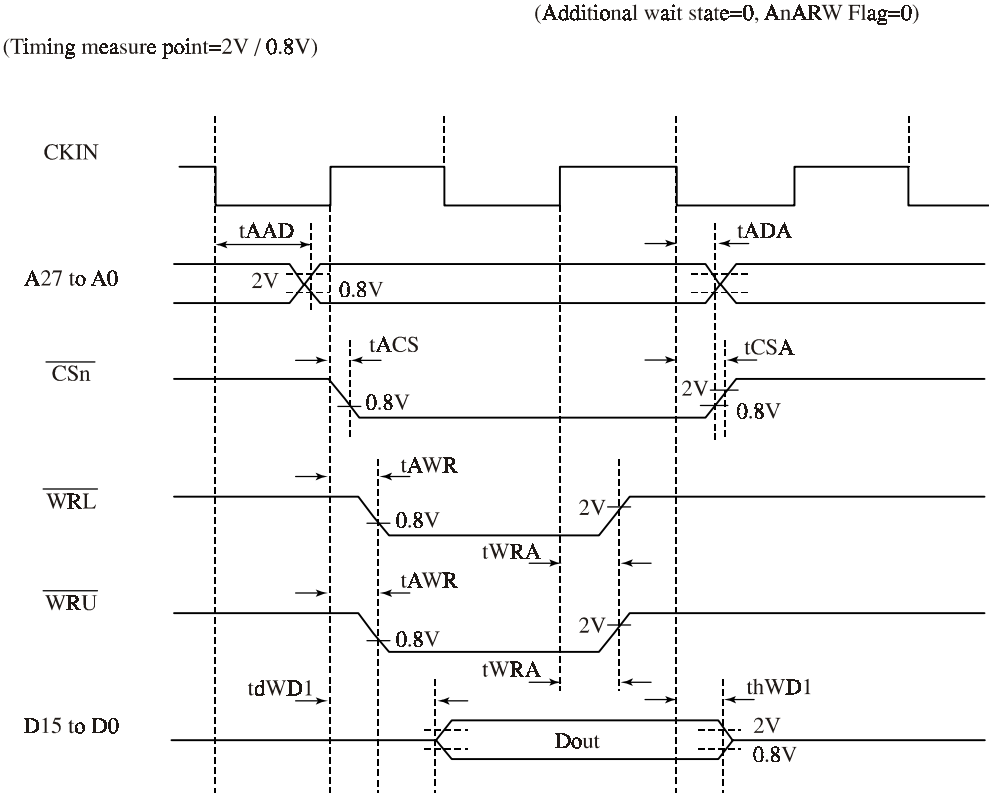


Figure9 DRAM Read Timing

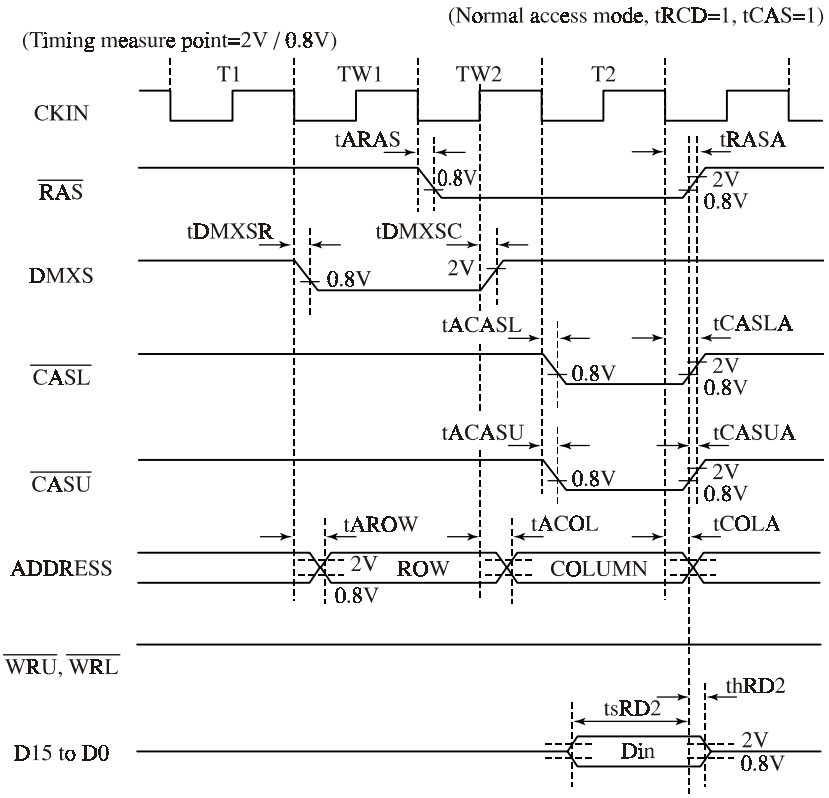


Figure10 DRAM Write Timing

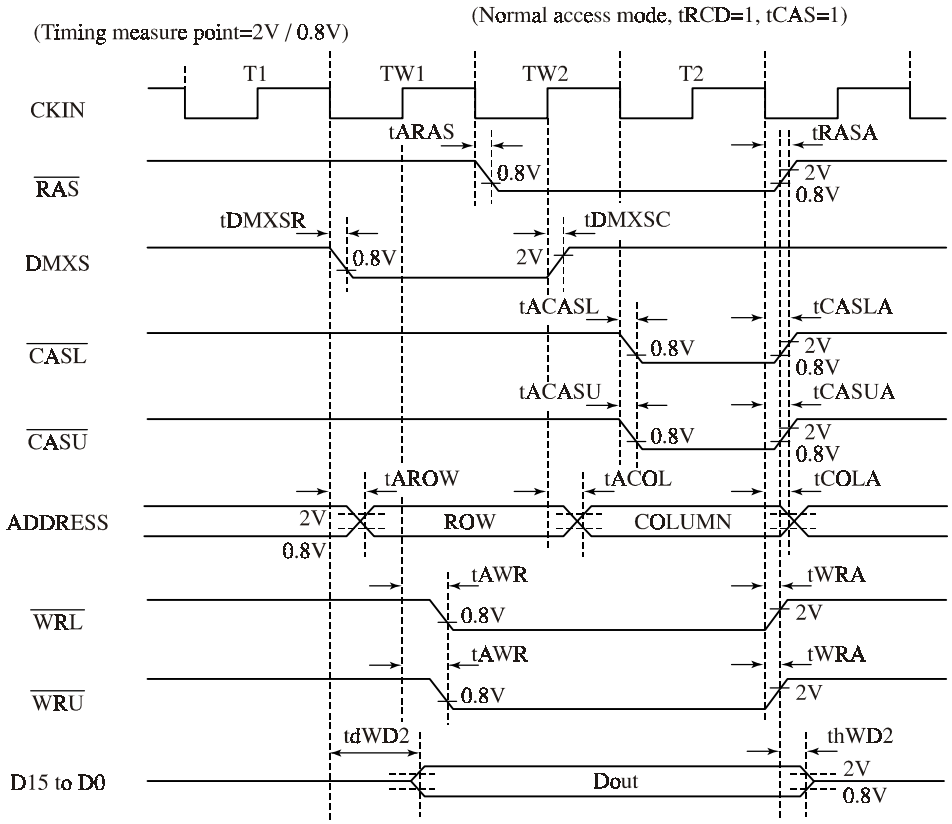


Figure11 REREQ Input/Output Timing

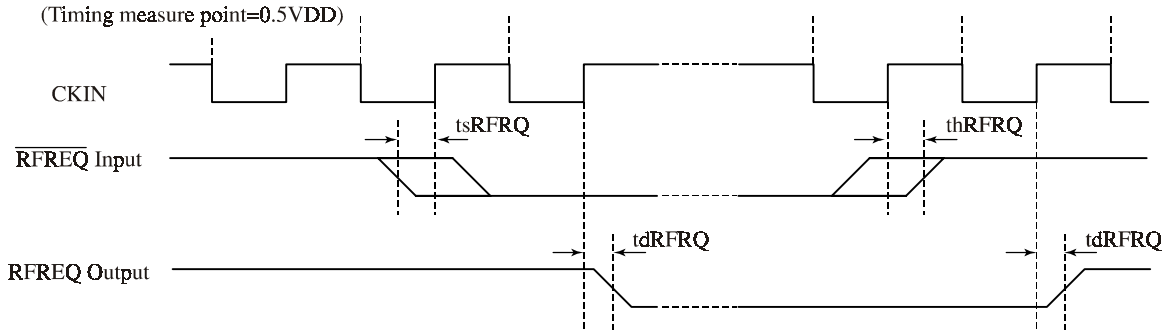


Figure12 Bus Request/Release Timing

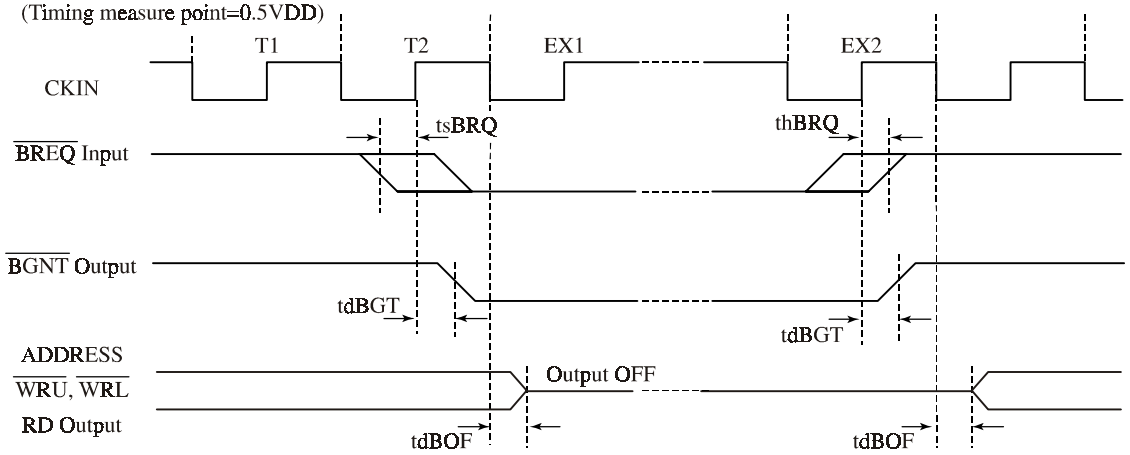


Figure13 Wait Input/Output Timing

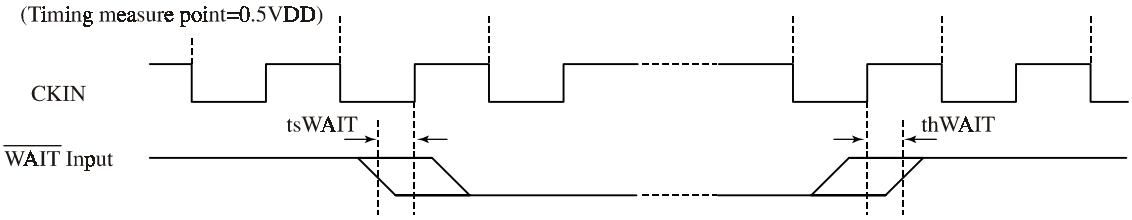


Figure14 The Load Used in Measuring the Timing