THOMSON SEMICONDUCTORS

EF9364A

EF9364B

CRT CONTROLER

The EF9364A/B is a CRT Controller which controls all of the functio associated with a 16 line x 64 character video display. Functions inclu CRT refresh, character entry, and cursor management.
The EF9364A/B contains an internal oscillator which produces the co posite sync output. The EF9364B generates a 60 Hz vertical sync wh the EF9364A generates a 50 Hz vertical sync.
Standard functions such as ERASE PAGE, ERASE LINE, and ERASE T END OF LINE make the EF9364A/B easy to interface to any computer o microprocessor, or to use as a stand-alone video processor.
The EF9364A/B requires only +5V power at less than 100 mA. It is ma factured in N channel silicon gate technology.

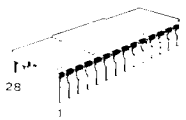
- Single +5V power supply
- 16 line x 64 character display
- On chip sync oscillator
- Complete cursor control
- Automatic scrolling
- Erase functions built in
- Performs character entry during horizontal sync
- Internal blinking cursor
- Page linking logic built in
- LS-TTL compatible

MOS

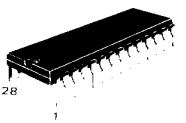
(N-CHANNEL, SILICON GATE)

CRT CONTROLLER

CASE CB-132

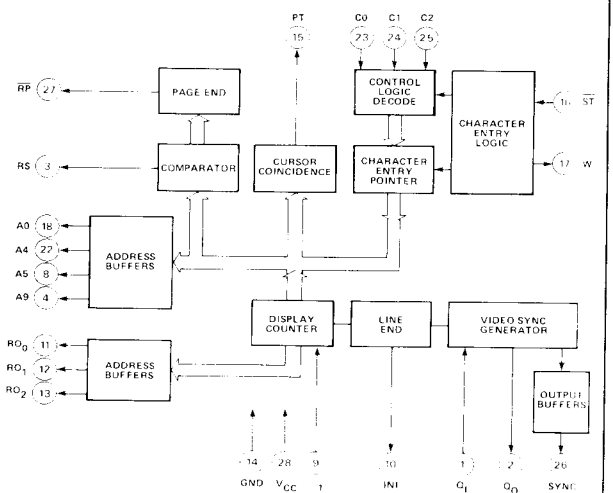


C SUFFIX
CERAMIC PACKAGE

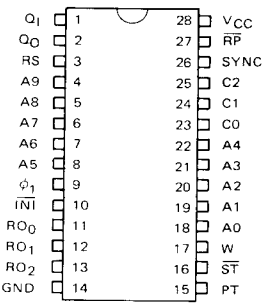


P SUFFIX
PLASTIC PACKAGE

BLOCK DIAGRAM



PIN ASSIGNMENT



NT 8110 A

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THOMSON COMPONENTS

• DESCRIPTION OF PIN FUNCTIONS

NAME	PIN NO	SYMBOL	FUNCTION
Crystal in Crystal out	1 2	Q_I Q_O	Pin one is the sync clock input. It may be driven directly from a TTL gate or from a parallel mode crystal connected between pins one and two. When a crystal is used, a 10 MΩ resistor should be connected in parallel. For standard 60 Hz line operation, a 1.018 MHz frequency source or crystal is required (with the EF9364B). For 50 Hz line operation, the EF9364A requires a 1.008 MHz crystal.
Page Select	3	RS	RS provides automatic page selection when two pages of memory are used. A «zero» output indicates selection of page 1; a logic «one» indicates page 2.
Memory Address	4-8	A9-A5	Upper order memory addresses lines ; A6-A9 determine which lines of text are being refreshed or written. A5 along with A0-A4 determine the character position.
Character Clock	9	ϕ_1	Character clock input. Addresses are changed on the trailing edge of ϕ_1.
Dot Clock Enable	10	$\overline{INT}$	A logic zero from $\overline{INT}$ used to inhibit oscillation of the dot clock for retrace blanking.
Row Address	11-13	RO_0 RO_1 RO_2	Character Generator row addresses. Blanks are generated by forcing RO_0-RO_2 to «000». During character entry, RO_2 gates data into memory to control the erase function. Row addressing follows the sequence 0-1-2-3-4-5-6-7-0-0-0-0- increment text line-0-1-2-etc.
Ground	14	GND	Ground.
Cursor	15	PT	Cursor video output. Indicates cursor location by a 2 Hz blinking underline.
Data Strobe	16	$\overline{ST}$	The rising edge of $\overline{ST}$ strobes the appropriate C0-C2 control word into the EF9364A/B.
Write	17	W	A positive going signal which indicates that the EF9364A/B is allowing a memory write. W is approximately 4 µs, and occurs during H sync. Memory address lines are latched at the cursor address during W.
Memory Address	18-22	A0-A4	Lower order memory addresses. A0-A4 plus A5 (pin 8) determine the character position.
Command Inputs	23-25	C0-C2	Command inputs are strobed into the EF9364A/B by $\overline{ST}$. Functions are as follows : **Function** — C_2 C_1 C_0 Page erase and cursor home (top-left) — 0 0 0 Erase to end of line and return cursor (to left) — 0 0 1 Line feed (cursor down) — 0 1 0 No operation* — 0 1 1 Cursor left (one position) — 1 0 0 Erasure of cursor-line — 1 0 1 Cursor up (one position) — 1 1 0 Normal character. Write signal is generated and cursor position is incremented — 1 1 1 * In order to suppress non displayed characters.
Composite Sync	26	SYNC	Positive logic composite sync output. Horizontal sync is generated during VSYNC and $\overline{VSYNC}$ time. A vertical sync output may be generated by logically «ANDing» SYNC and $\overline{INT}$.
End of Page	27	$\overline{RP}$	This output is used to increment an external page counter when using more than one page of memory.
Power Supply	28	V_{CC}	+ 5 volt supply.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Voltage on any pin, with respect to ground	V_{in}, V_{out}	−0.3 to +7.0	Vdc
Operating temperature range	T_A	0 to +70	°C
Storage temperature range	T_{stg}	−65 to +150	°C

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

ELECTRICAL CHARACTERISTICS

($T_A = 0°C$ to $+70°C$, $V_{cc} = 5.0$ V ± 5%, unless otherwise noted)

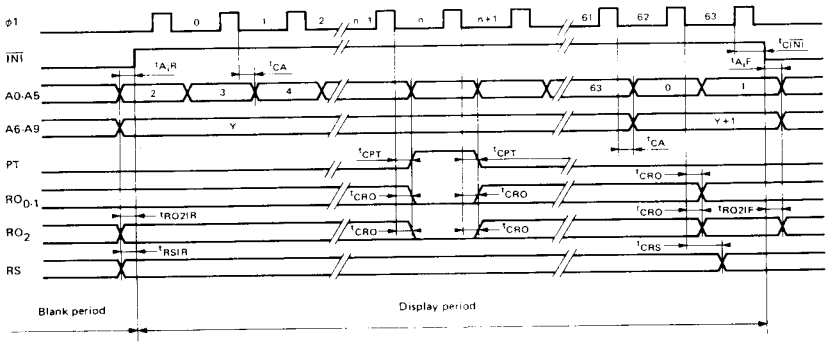
DC CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Input voltage levels - (except $\phi 1$)					
Low level	V_{IL}	–	–	0.65	Vdc
High level	V_{IH}	2.2	–	–	Vdc
Input voltage levels - $\phi 1$					
Low level	V_{IL}	–	–	0.65	Vdc
High level	V_{IH}	3.5	–	–	Vdc
Output voltage levels - ($\overline{INT}$ only)					
Low level $I_{OL} = 1.9$ mA	V_{OL}	–	–	0.4	Vdc
High level $I_{OH} = -100\ \mu A$	V_{OH}	2.2	–	–	Vdc
Output voltage levels - (except $\overline{INT}$)					
Low level $I_{OL} = 0.36$ mA	V_{OL}	–	–	0.4	Vdc
High level $I_{OH} = -100\ \mu A$	V_{OH}	2.2	–	–	Vdc
Input current					
Low level $0 \leq V_{in} \leq +5$ V	I_{IL}	–	–	10	μA
Input capacitance	C_{in}				
All inputs - (except $\phi 1$) $V_{in} = GND$		–	5	7	pF
$\phi 1$ only $V_{in} = GND$		–	17	25	pF
Power supply current	I_{CC}	–	100	120	mA

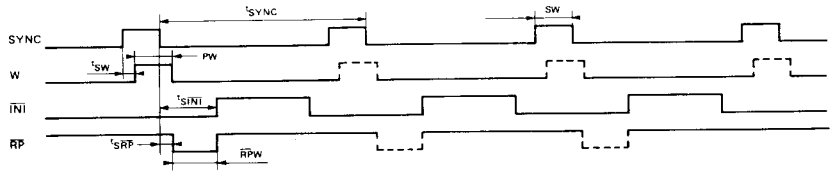
AC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Frequency of control clock $\phi 1$	$f\phi$	–	1.6	–	MHz
Crystal frequency EF9364A	f_x	–	1.008	–	MHz
EF9364B		–	1.018	–	MHz
$\phi 1$ pulse width	$t_{w\phi}$	200	–	–	ns
Rise and fall times	$t_{r\phi}$ $t_{f\phi}$	–	20	40	ns
Refresh memory address access time	t_{CA}	–	200	250	ns
Character memory address access time	t_{CRO}	–	200	250	ns
RS access time (Read)	t_{CRS}	–	300	1000	ns
PT access time	t_{CPT}	–	200	250	ns
$\overline{INT}$ access time (high to low)	$t_{C\overline{INT}}$	–	100	150	ns
SYNC period	t_{SYNC}	–	64	–	μs
SYNC pulse width	SW	–	4	–	μs
$\overline{INT}$ access time (low to high)	$t_{S\overline{INT}}$	–	11	–	μs
$\overline{RP}$ access time (high to low)	$t_{S\overline{RP}}$	–	1	1.5	μs
W access time (low to high)	t_{SW}	–	500	1000	ns
W pulse width	PW	–	4	–	μs
$\overline{RP}$ pulse width	$\overline{RPW}$	–	10	–	μs
Address to rising edge of $\overline{INT}$	t_{A_iR}	0	–	2.1	μs
Falling edge of $\overline{INT}$ to address delay	t_{A_iF}	0	–	1	μs
Row to rising edge of $\overline{INT}$ delay	t_{RO2IR}	0	–	2.1	μs
Falling edge of $\overline{INT}$ to row delay	t_{RO2IF}	0	–	1	μs
RS to rising edge of $\overline{INT}$ delay	t_{RSIR}	0	–	–	μs

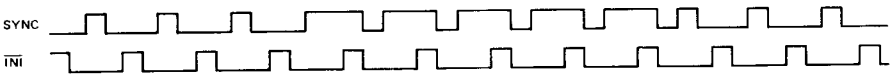
LINE TIMING



SYNC TIMING



FRAME TIMING



DATA INPUT TIMING

Asynchronous Operation

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{ST}$ Pulse Width	$\overline{STW}$	0.5			μs
C0-C2 Set Up Time	$t_{C\overline{ST}}$	1	–	–	μs
C0-C2 Hold Time	$t_{\overline{STC}}$	78	–	–	μs

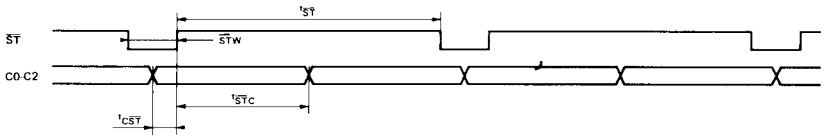
Minimum Strobe period $t_{\overline{ST}}$ (Operation excution time)

FUNCTION	CONTROL INPUTS			Max Execution Time	Unit
	C2	C1	C0		
Page Erase & Cursor Home	0	0	0	132	ms
Erase to End of Line & Return Cursor	0	0	1	4.2	ms
Line Feed (Cursor Down)	0	1	0	130*	μs
No Operation	0	1	1	80	μs
Cursor Left	1	0	0	80	μs
Erasure of Cursor Line	1	0	1	8.3	ms
Cursor Up	1	1	0	80	μs
Normal Character	1	1	1	130*	μs

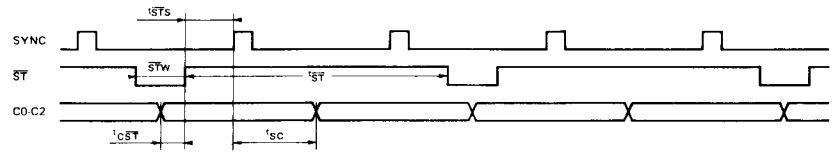
* Will increase to 8.3 ms when text scroll occurs. See «Scrolling» for conditions.

DATA INPUT TIMING

Asynchronous operation



Synchronous operation



Synchronous Operation

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{ST}$ Pulse Width	$\overline{STW}$	0.5	–	–	µs
C0-C2 Set Up Time (from $\overline{ST}$)	$t_{C\overline{ST}}$	1	–	–	µs
C0-C2 Hold time (from SYNC)	t_{SC}	16	–	–	µs
$\overline{ST}$ Set Up Time (from SYNC)	$t_{\overline{ST}S}$	1	–	–	µs

Minimum Strobe Period $t_{\overline{ST}}$ (Operation execution time)

FUNCTION	CONTROL INPUTS			Max Execution time	Unit
	C2	C1	C0		
Page Erase & Cursor Home	0	0	0	132	ms
Erase to End of Line & Return Cursor	0	0	1	4.2	ms
Line Feed (Cursor Down)	0	1	0	80*	µs
No Operation	0	1	1	80	µs
Cursor Left	1	0	0	80	µs
Erasure of Cursor Line	1	0	1	8.3	ms
Cursor Up	1	1	0	80	µs
Normal Character	1	1	1	80	µs

*Will increase to 8.3 ms when text scroll occurs. See «Scrolling» for conditions.

OPERATION

The EF9364A/B provides all of the control functions required by a CRT display with a minimum of external circuitry.
The cursor and erase commands may be decoded from the data bus by a low cost 256 x 4 PROM.
The EF9364A/B then provides the necessary cursor movement and gates the memory for writing or erasing. Erase is controlled by providing a write signal to RAM, and gating «zeros» to the RAM input bus. Use of an external PROM allows user selection of control words.
The RAM write command, «W», is generated during horizontal retrace. At this time, the RAM address is set to the cursor address. Immediately following the write command, the RAM addresses revert to refresh addressing and the cursor is shifted one character.

CURSOR

The cursor location is indicated by an alternating high on pin 15 (PT) at row 7, and a low on pin 15 with RO_0-RO_2 forced low at rows 0-6. These alternate at a 2 Hz rate. If PT is used to force the display on, the result will be a blink of the cursor character position alternating with an underline at a 2 Hz rate.

CHARACTER ENTRY

When a Normal Character code (C2, C1, C0 = 1, 1, 1) and a Data Strobe are received, the write command will be generated during horizontal retrace. If, at the end of the horizontal retrace, the cursor is at the last position on a line, a carriage return and line feed will automatically occur. When the cursor is at the last position of the last line, a carriage return and up-scroll will automatically occur.

SCROLLING

Scrolling of the screen text will occur under any of the following characteristics :

1. Inputting a line feed command when the cursor is at the bottom line of the screen.
2. Inputting a character when the cursor is at the bottom right hand side of the screen.

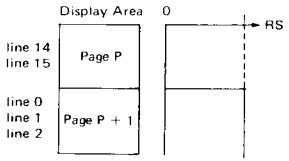
Scrolling will result in the entire top line of the screen being erased and all of the remaining lines shifting up. Alternatively, a Roll (defined as all of the lines shifting up with the previous top line reappearing at the bottom of the screen) may be performed by inhibiting the write signal to the page memory as described in «Extra Functions.»

EXTRA FUNCTIONS

By using the fourth bit of the decoder PROM as a write enable signal, and properly programming the PROM, the additional commands of Home Cursor, Return Cursor, and Roll Screen may be generated. This is done by inhibiting the W signal to the page memory and inputting the control codes, respectively, of Page Erase and Home Cursor, Erase to end of line and Return Cursor, and Line Feed.

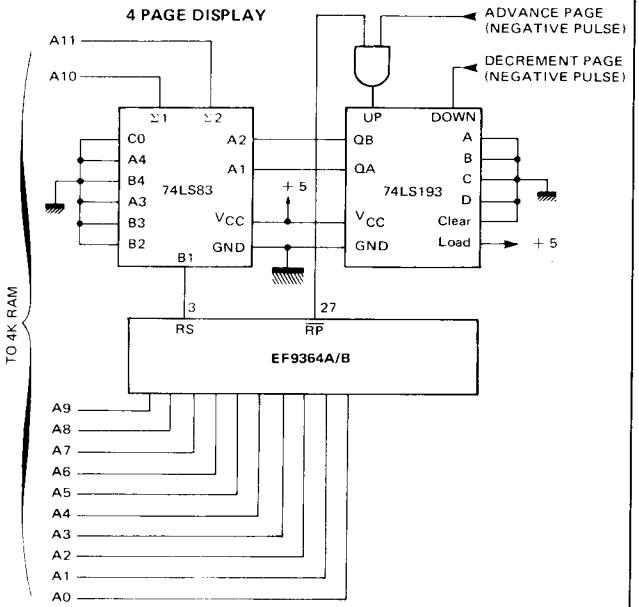
MULTIPLE PAGE DISPLAY

When linking two or more pages, the $\overline{RP}$ and RS signals may be used to allow a «moving window» text display.
RS (Page Select) indicates the end of page location. If a scroll has occurred, RS will show the transition from the end of line 15 of page P and the beginning of line 0 of page P + 1.

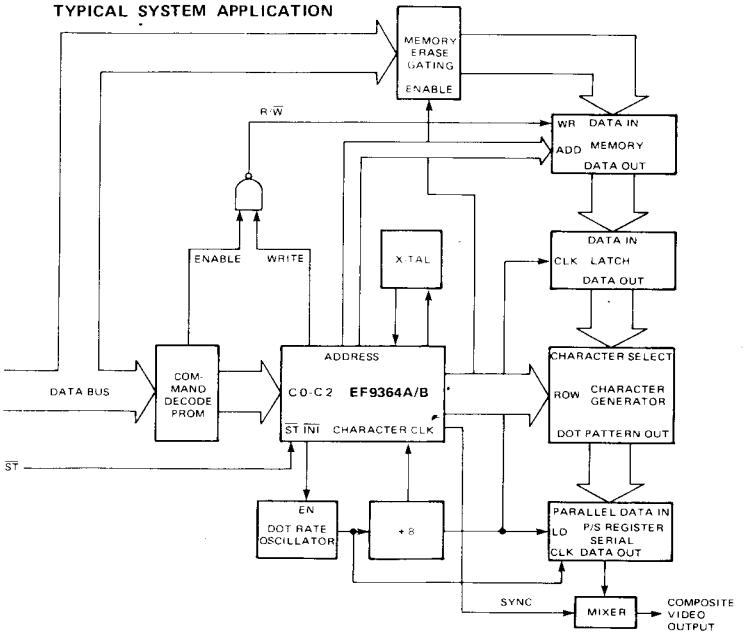


To properly maintain the memory address when displaying more than two pages, $\overline{RP}$ pulses low at the point in time when page P is scrolled completely off the screen. At this time, RS will remain low for the entire frame since page P + 1 is now the only displayed page. The circuit at the right will allow scrolling through 4 pages of memory.

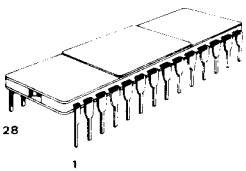
4 PAGE DISPLAY



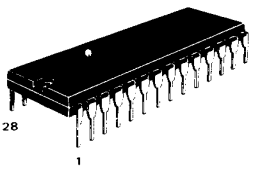
TYPICAL SYSTEM APPLICATION



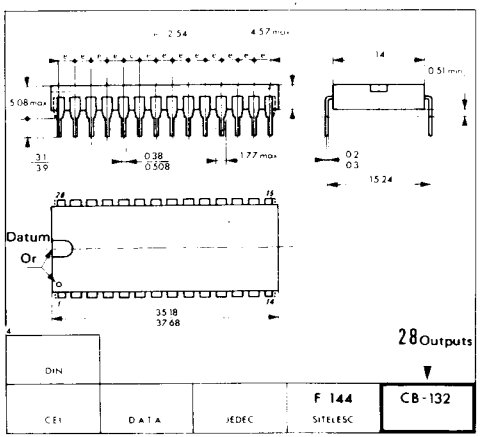
CASE CB-132



C SUFFIX
CERAMIC PACKAGE



P SUFFIX
PLASTIC PACKAGE



These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.