65,536-WORD BY 4-BIT DYNAMIC RANDOM-ACCESS MEMORY

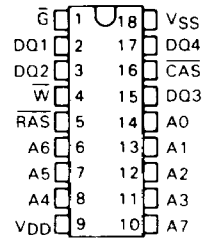
SEPTEMBER 1987 – REVISED NOVEMBER 1989

- 65,536 × 4 Organization
- Single 5-V Supply (10% Tolerance)
- JEDEC Standardized Pinout
- Pinout Identical to SMJ4416 (16K × 4 Dynamic RAM)
- Performance Ranges:

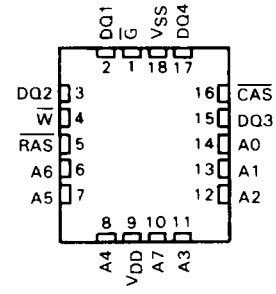
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE CYCLE (MIN)
SMJ4464-12	120 ns	60 ns	230 ns	320 ns
SMJ4464-15	150 ns	75 ns	260 ns	345 ns
SMJ4464-20	200 ns	100 ns	330 ns	435 ns

- Long Refresh Period . . . 4 ms (Max)
- Low Refresh Overhead Time . . . As Low As 1.3% of Total Refresh Period
- On-Chip Substrate Bias Generator
- All Inputs, Outputs, and Clocks Fully TTL Compatible
- 3-State Unlatched Output
- Early Write or $\overline{G}$ to Control Output Buffer Impedance
- Page-Mode Operation for Faster Access
- Power Dissipation As Low As:
  - Operating . . . 275 mW (Typ)
  - Standby . . . 12.5 mW (Typ)
- $\overline{RAS}$-Only Refresh Mode
- $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Mode

JD PACKAGE
(TOP VIEW)



FV PACKAGE
(TOP VIEW)



NOTE: Pin 1 indicator on back

PIN NOMENCLATURE	
A0 A7	Address Inputs
$\overline{CAS}$	Column-Addreess Strobe
DQ1 DQ4	Data In Data Out
$\overline{G}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5 V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The SMJ4464 is a high-speed, 262,144-bit dynamic random-access memory, organized as 65,536 words of four bits each. It employs state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon/polycide gate technology for very high performance combined with low cost and improved reliability.

This device features maximum $\overline{RAS}$ access times of 120 ns, 150 ns, or 200 ns. Typical power dissipation is as low as 275 mW operating and 12.5 mW standby.

New SMOS technology permits operation from a single 5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{DD} peaks of 125 mA are typical, and a −0.7-V input voltage undershoot can be tolerated, minimizing system noise considerations.

All inputs and outputs, including clocks, are compatible with Series 54 TTL. All address and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The SMJ4464 is offered in 18-pin 300-mil ceramic side-braze dual-in-line and 18-pad leadless ceramic chip carrier packages. It is guaranteed for operation from −55°C to 110°C for the S version and from 0°C to 70°C for the L version. The dual-in-line package is designed for insertion in mounting-hole rows on 7,62-mm (300-mil) centers).

operation

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data out will remain in the high-impedance state for the entire cycle, permitting common I/O operation.

data in (DQ1-DQ4)

Data is written during a write or a read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or a read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In a delayed or read-modify write cycle, $\overline{G}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

data out (DQ1-DQ4)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fanout of two Series 54 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ and $t_{a(G)}$ are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{G}$ are low. $\overline{CAS}$ or $\overline{G}$ going high returns it to a high-impedance state. In a delayed-write or read-modify-write cycle, the output must be put in the high-impedance state prior to applying data to the DQ input. This is accomplished by bringing $\overline{G}$ high prior to applying data, thus satisfying t_{GHD}.

output enable ($\overline{G}$)

The $\overline{G}$ input controls the impedance of the output buffers. When $\overline{G}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{G}$ low during a normal cycle will activate the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state. Once in the low-impedance state they will remain in the low-impedance state until $\overline{G}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every four milliseconds to retain data. This can be achieved by strobing each of the 256 rows (A0-A7). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state.

operation (continued)

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh

The $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh is utilized by bringing $\overline{\text{CAS}}$ low earlier than $\overline{\text{RAS}}$ (see parameter t_{CLRL}) and holding it low after $\overline{\text{RAS}}$ falls (see parameter t_{RLCHR}). For successive $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycles, $\overline{\text{CAS}}$ can remain low while cycling $\overline{\text{RAS}}$. The external address is ignored and the refresh address is generated internally.

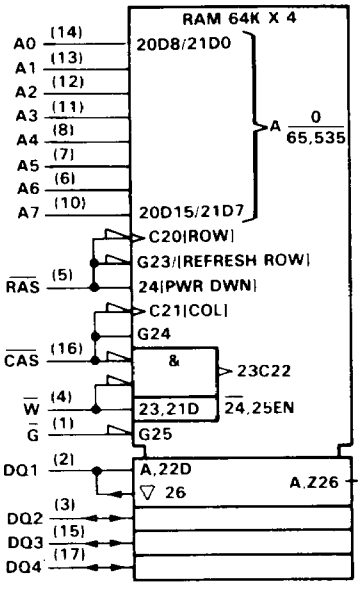
page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing random column addresses onto the chip. Thus, the time required to set up and strobe sequential row addresses for the same page is eliminated. The maximum number of columns that can be addressed is determined by $t_{W(RL)}$, the maximum $\overline{\text{RAS}}$ low pulse duration.

power up

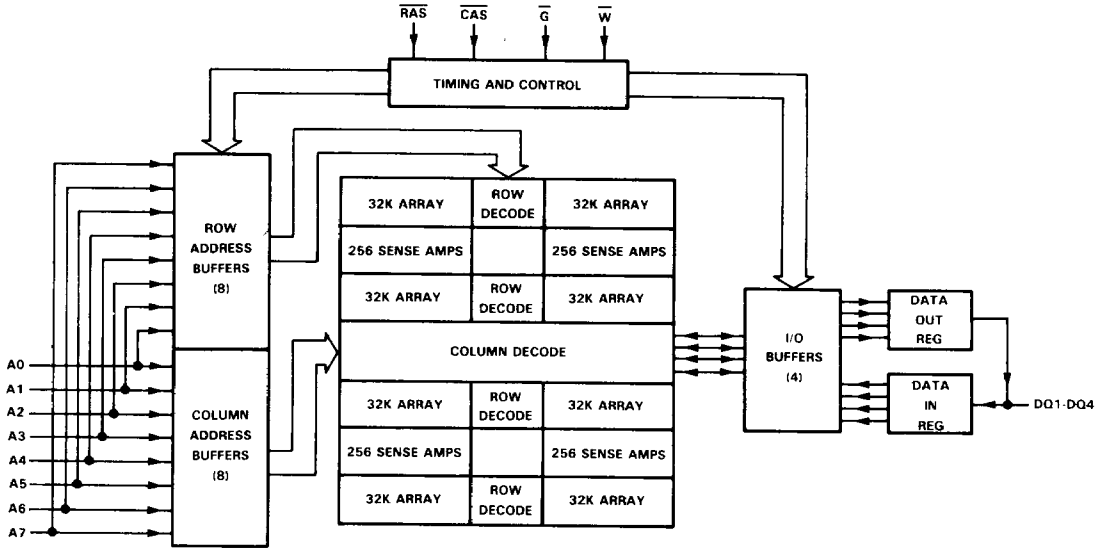
To achieve proper device operation, an initial pause of 200 μs is required after power up, followed by a minimum of eight initialization cycles.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the dual-in-line package.

functional block diagram



absolute maximum ratings over operating temperature range (unless otherwise noted)†

Voltage on any pin including V_{DD} supply (see Note 1) . . . . . −1 V to 7 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Minimum operating free-air temperature: S version . . . . . −55°C
L version . . . . . 0°C
Maximum operating case temperature: S version . . . . . 110°C
L version . . . . . 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		S VERSION			L VERSION			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{DD}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{SS}	Supply voltage		0			0		V
V_{IH}	High-level input voltage	2.4		$V_{DD}+0.3$	2.4		$V_{DD}+0.3$	V
V_{IL}	Low-level input voltage (see Note 2)	−0.7		0.7	−0.7		0.7	V
T_A	Operating free-air temperature	−55			0			°C
T_C	Operating case temperature			110			70	°C

NOTE 2: The algebraic convention, where the negative (less positive) limit is designated as maximum, is used in this data sheet for logic voltage levels only.

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electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SMJ4464-12			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All outputs open			±10	μA
I_O	Output current (leakage)	V_O = 0 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		65	80	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		2.5	8	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high, All outputs open		50	60	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, All outputs open		45	55	mA

PARAMETER		TEST CONDITIONS	SMJ4464-15			SMJ4464-20			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All outputs open			±10			±10	μA
I_O	Output current (leakage)	V_O = 0 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		55	70		50	60	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		2.5	8		2.5	8	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high, All outputs open		45	55		40	50	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, All outputs open		40	50		30	40	mA

†All typical values are at T_A = 25°C and nominal supply voltages.

capacitance over recommended supply voltage range and operating temperature range, f = 1 MHz‡

PARAMETER		SMJ4464			UNIT
		MIN	TYP†	MAX	
$C_{i(A)}$	Input capacitance, address inputs		4	6	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		6	8	pF
$C_{i(W)}$	Input capacitance, write enable input		6	8	pF
$C_{i/o}$	Output capacitance		7	8	pF

†All typical values are at T_A = 25°C and nominal supply voltages.
‡V_{CC} equal to 5.0 V and the bias on pins under test is 0.0 V

switching characteristics over recommended supply voltage range and operating temperature range

PARAMETER		TEST CONDITIONS§	ALT. SYMBOL	SMJ4464-12		UNIT
				MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{RLCL} \geq$ MAX, C_L = 80 pF, I_{OH} = −5 mA, I_{OL} = 4.2 mA	t_{CAC}		60	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 80 pF, I_{OH} = −5 mA, I_{OL} = 4.2 mA	t_{RAC}		120	ns
$t_{a(G)}$§	Access time after $\overline{G}$ low	C_L = 80 pF, I_{OH} = −5 mA, I_{OL} = 4.2 mA	t_{GAC}		35	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 80 pF, I_{OH} = −5 mA, I_{OL} = 4.2 mA	t_{OFF}	0	30	ns
$t_{dis(G)}$	Output disable time after $\overline{G}$ high	C_L = 80 pF, I_{OH} = −5 mA, I_{OL} = 4.2 mA	t_{GOFF}	0	38	ns

switching characteristics over recommended supply voltage range and operating temperature range

PARAMETER		TEST CONDITIONS§	ALT. SYMBOL	SMJ4464-15		SMJ4464-20		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{RLCL} \geq$ MAX, C_L = 80 pF, I_{OH} = −5 mA, I_{OL} = 4.2 mA	t_{CAC}		75		100	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 80 pF, I_{OH} = −5 mA, I_{OL} = 4.2 mA	t_{RAC}		150		200	ns
$t_{a(G)}$¶	Access time after $\overline{G}$ low	C_L = 80 pF, I_{OH} = −5 mA, I_{OL} = 4.2 mA	t_{GAC}		45		55	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 80 pF, I_{OH} = −5 mA, I_{OL} = 4.2 mA	t_{OFF}	0	30	0	35	ns
$t_{dis(G)}$	Output disable time after $\overline{G}$ high	C_L = 80 pF, I_{OH} = −5 mA, I_{OL} = 4.2 mA	t_{GOFF}	0	38	0	38	ns

§ Figure 1 shows the load circuit; C_L values shown are typical for test system used.
¶$t_{a(C)}$ and $t_{a(R)}$ must be satisfied to guarantee $t_{a(G)}$.

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timing requirements over recommended supply voltage range and operating temperature range

		ALT. SYMBOL	SMJ4464-12 MIN	SMJ4464-12 MAX	UNIT
$t_{c(P)}$	**Page-mode cycle time**†	t_{PC}	120		ns
$t_{c(PM)}$	**Page-mode cycle time (read-modify-write cycle)**†	t_{PCM}	205		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	230		ns
$t_{c(W)}$	**Write cycle time**†	t_{WC}	230		ns
$t_{c(rdW)}$	**Read-write/read-modify-write cycle time**†	t_{RWC}	320		ns
$t_{w(CH)P}$	Pulse duration, $\overline{CAS}$ high (page mode)	t_{CP}	50		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (non-page mode)	t_{CPN}	50		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low‡	t_{CAS}	60	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low§	t_{RAS}	120	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	40		ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		ns
$t_{su(D)}$	Data setup time	t_{DS}	10		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		ns
$t_{su(WCL)}$	Early-write command setup time before $\overline{CAS}$ low	t_{WCS}	0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	40		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	40		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	20		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	80		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	35		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	95		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	35		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	35		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	95		ns
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high¶	t_{CHR}	25		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	120		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low¶	t_{RCP}	0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	60		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)#	t_{CWD}	100		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low¶	t_{CSR}	25		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	60	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)#	t_{RWD}	160		ns
t_{GHD}	Delay time, $\overline{G}$ high before data applied at DQ	t_{GDD}	25		ns
t_{rf}	Refresh time interval	t_{REF}		4	ms

† All cycle times assume t_t = 5 ns.
‡ In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$).
§ In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).
¶ $\overline{CAS}$-before-$\overline{RAS}$ refresh option only.
# $\overline{G}$ must disable the output buffers prior to applying data to the device.
NOTE 3: System transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ are to be a minimum of 3 ns and a maximum of 50 ns.

timing requirements over recommended supply voltage range and operating temperature range

		ALT. SYMBOL	SMJ4464-15 MIN	SMJ4464-15 MAX	SMJ4464-20 MIN	SMJ4464-20 MAX	UNIT
$t_{c(P)}$	**Page-mode cycle time**†	t_{PC}	145		190		ns
$t_{c(PM)}$	**Page-mode cycle time (read-modify-write cycle)**†	t_{PCM}	230		295		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	260		330		ns
$t_{c(W)}$	**Write cycle time**†	t_{WC}	260		330		ns
$t_{c(rdW)}$	**Read-write/read-modify-write cycle time**†	t_{RWC}	345		435		ns
$t_{w(CH)P}$	Pulse duration, $\overline{CAS}$ high (page mode)	t_{CP}	60		80		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (non-page mode)	t_{CPN}	60		80		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low‡	t_{CAS}	75	10,000	100	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	100		120		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low§	t_{RAS}	150	10,000	200	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	45		55		ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	10		10		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Early-write command setup time before $\overline{CAS}$ low	t_{WCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	45		60		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	45		60		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	25		45		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		20		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	100		145		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	45		55		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	120		155		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	45		55		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		15		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	45		55		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	120		155		ns
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high¶	t_{CHR}	30		35		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low¶	t_{RCP}	10		15		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	75		100		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)#	t_{CWD}	110		140		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low¶	t_{CSR}	30		35		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	75	30	100	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)#	t_{RWD}	185		240		ns
t_{GHD}	Delay time, $\overline{G}$ high before data applied at DQ	t_{GDD}	25		35		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

† All cycle times assume t_t = 5 ns.
‡ In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$).
§ In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).
¶ $\overline{CAS}$-before-$\overline{RAS}$ refresh option only.
# $\overline{G}$ must disable the output buffers prior to applying data to the device.
NOTE 3: System transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ are to be a minimum of 3 ns and a maximum of 50 ns.

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PARAMETER MEASUREMENT INFORMATION

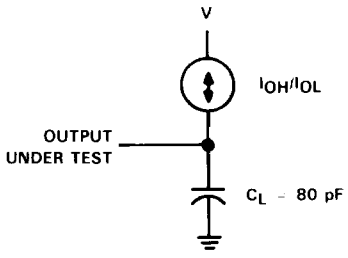
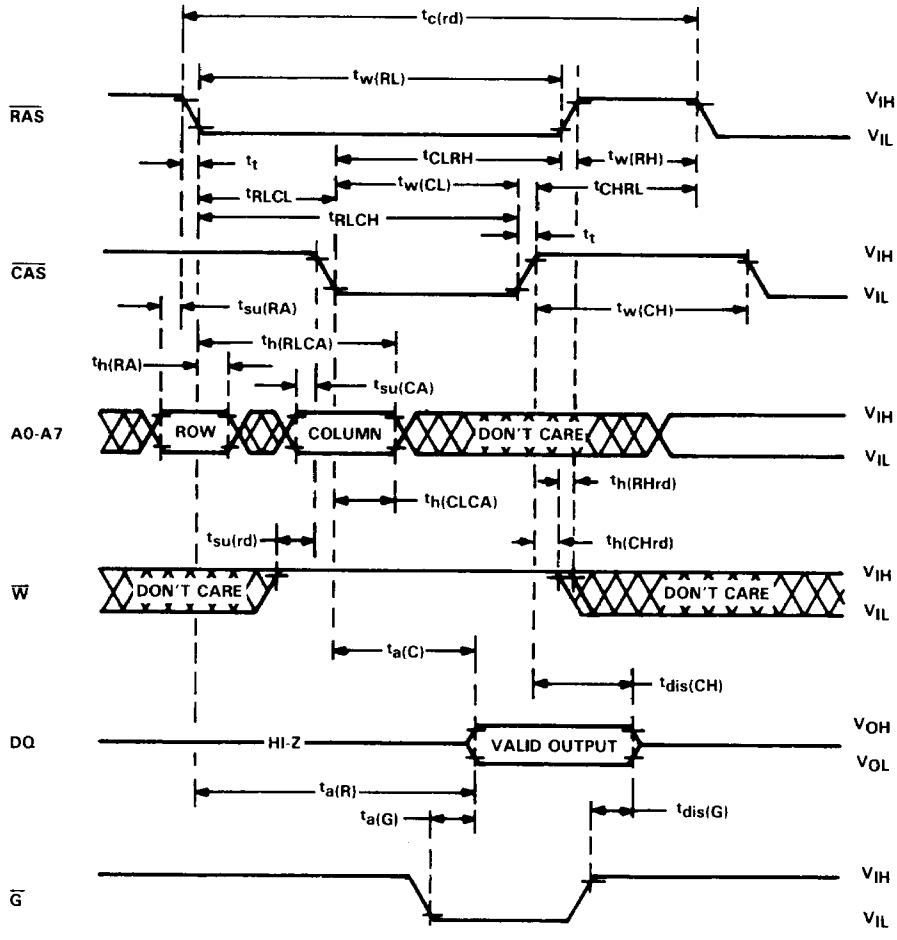


FIGURE 1. TYPICAL LOAD CIRCUIT

read cycle timing



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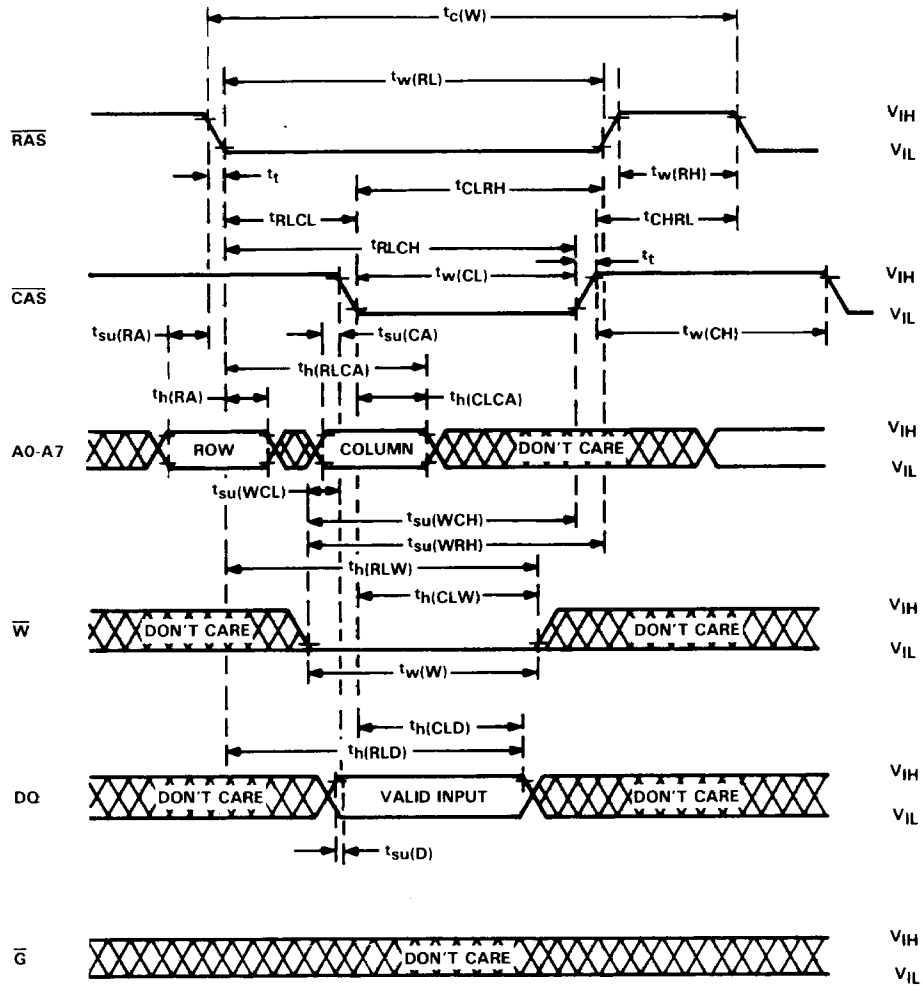
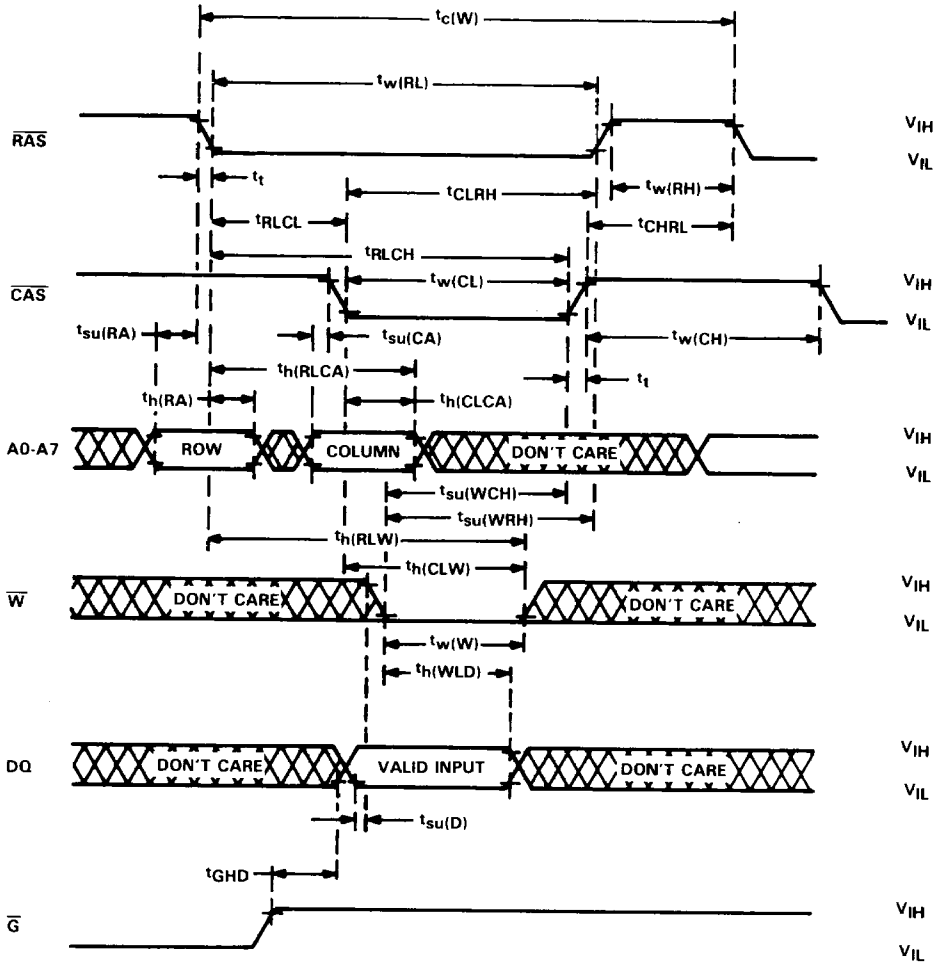
early write cycle timing



write cycle timing



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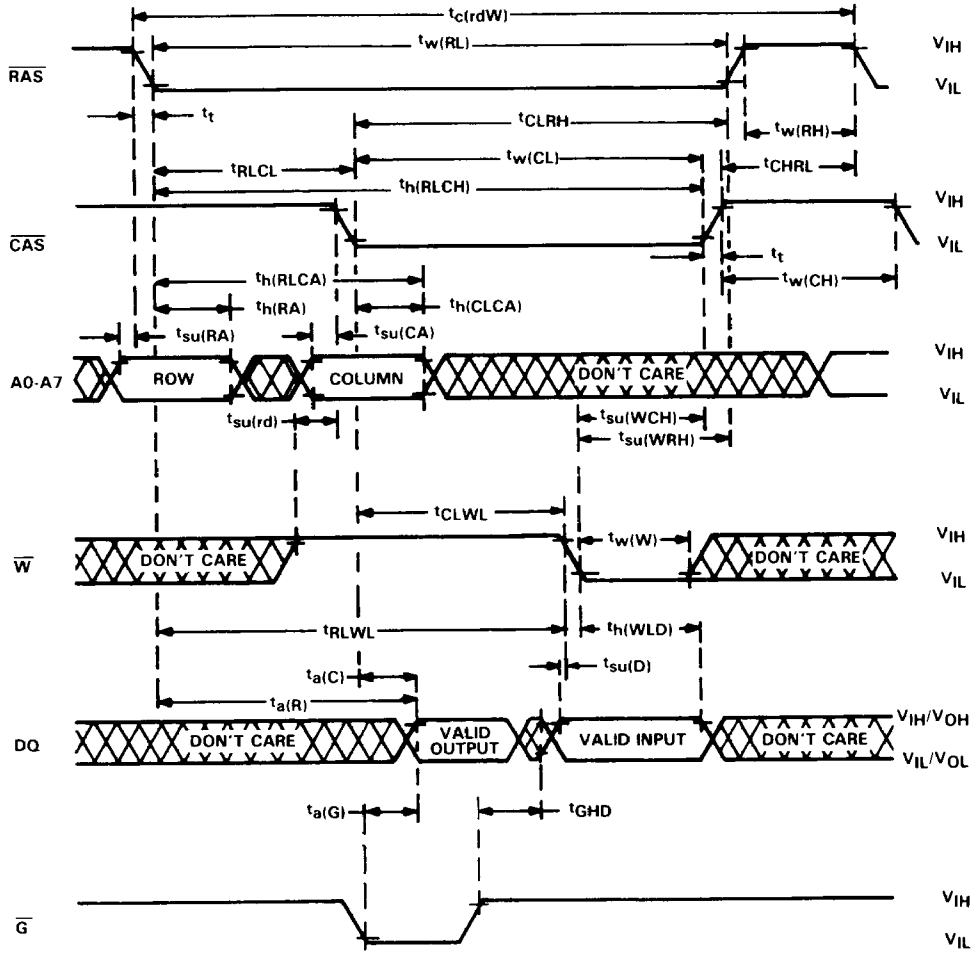
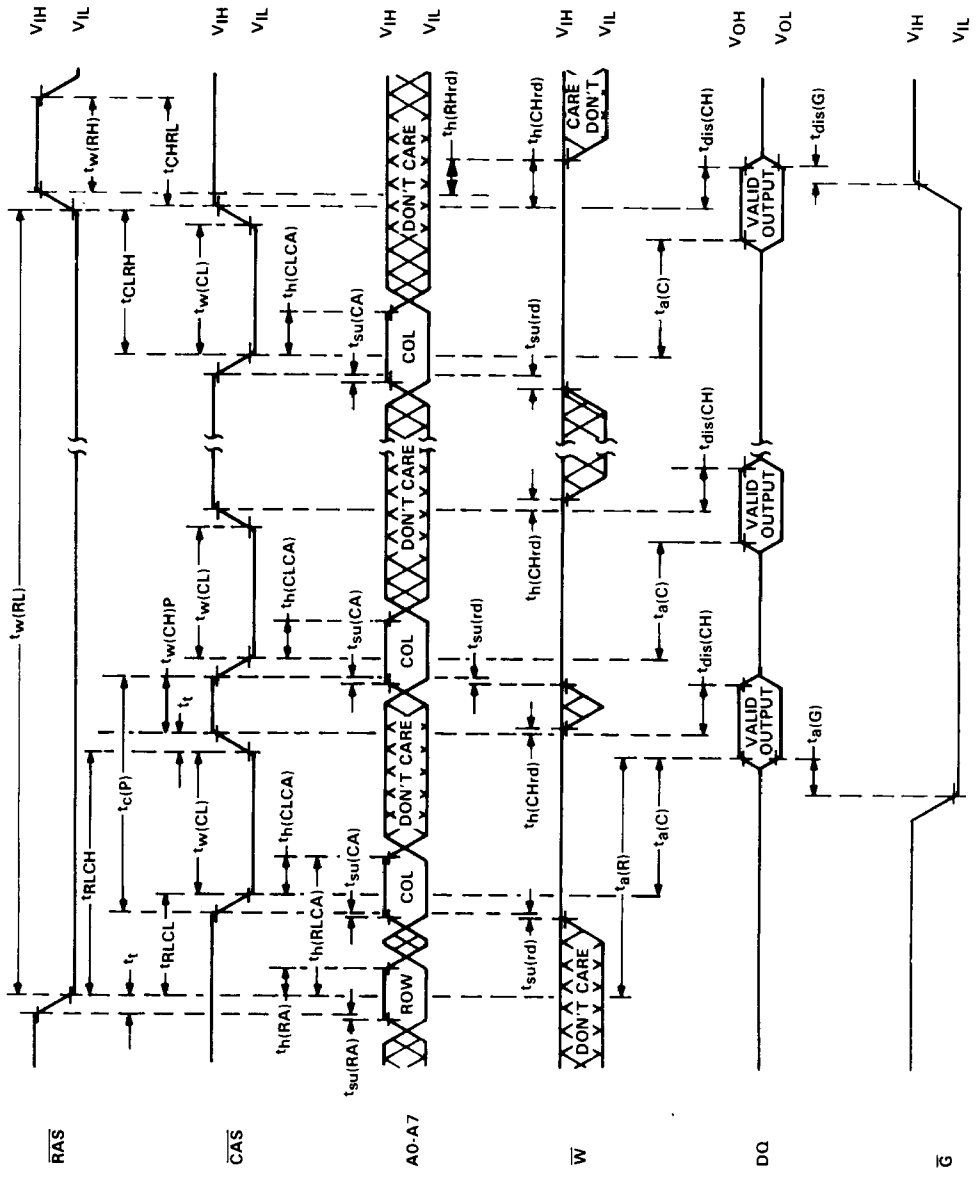
read-write/read-modify-write cycle timing



page-mode read cycle timing



NOTE 4: A write cycle or read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

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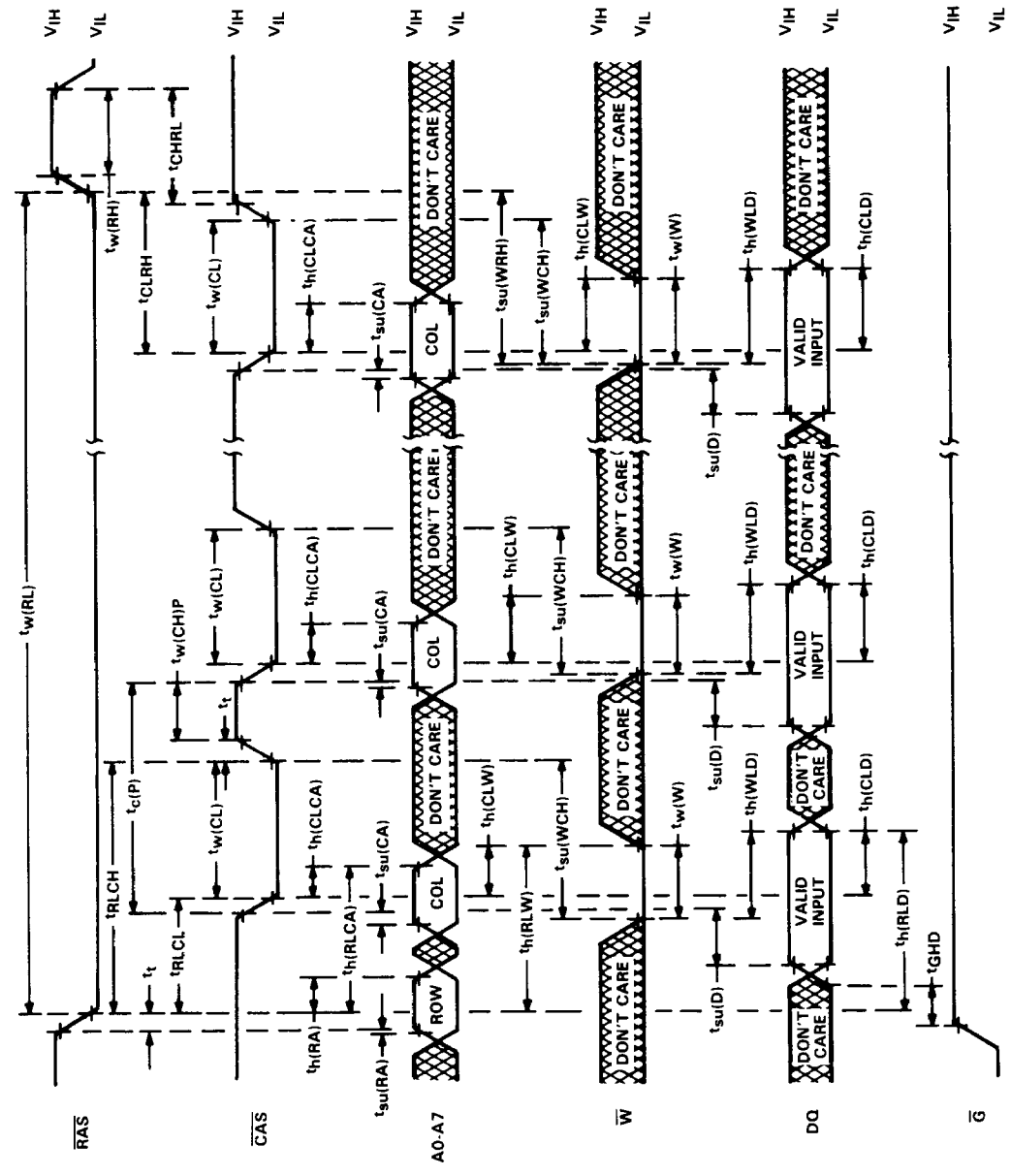
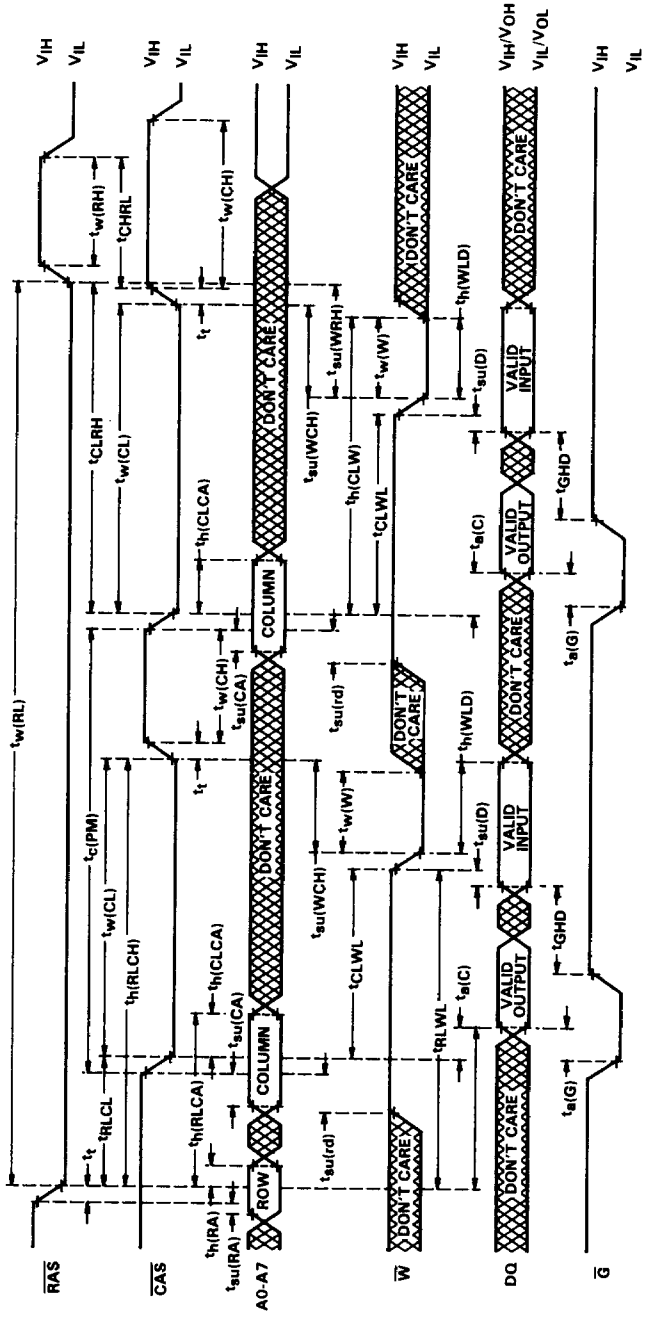
page-mode write cycle timing



NOTE 5: A read cycle or read-modify-write cycle can be intermixed with write cycles as long as the read and read-modify-write timing specifications are not violated.

page-mode read-modify-write cycle timing



NOTE 6: A read cycle or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

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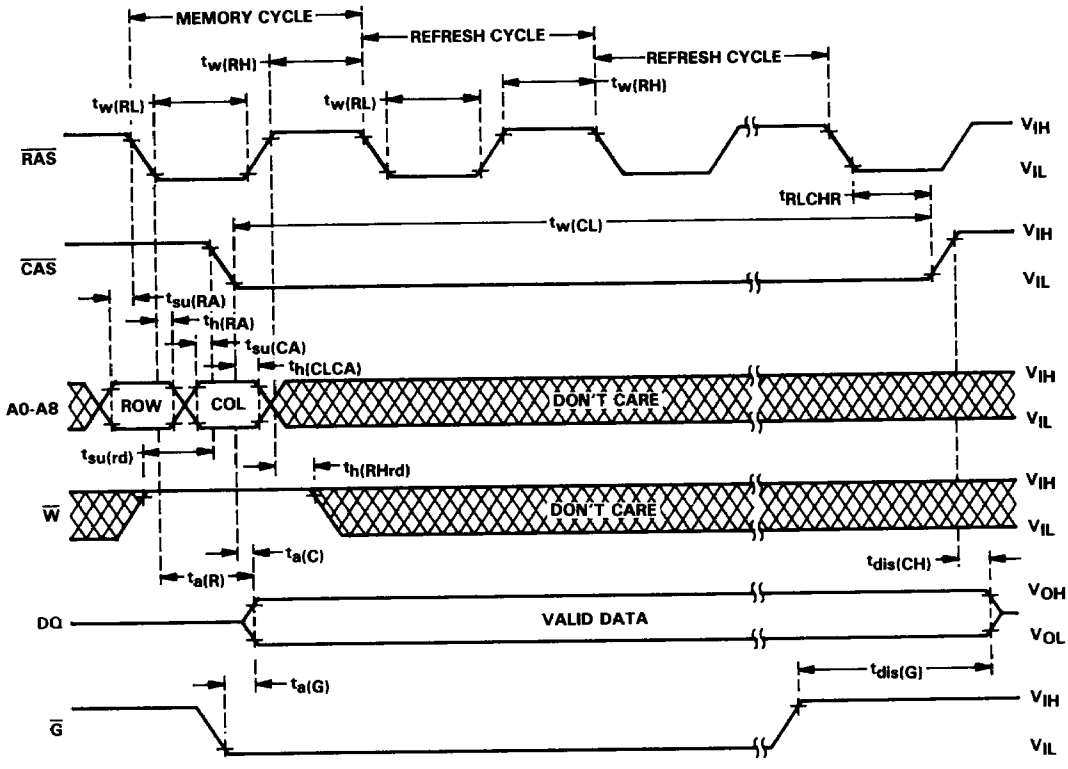
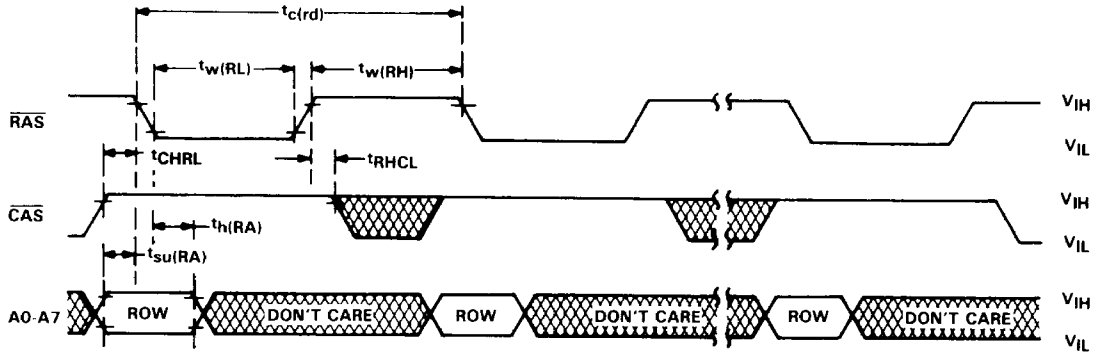
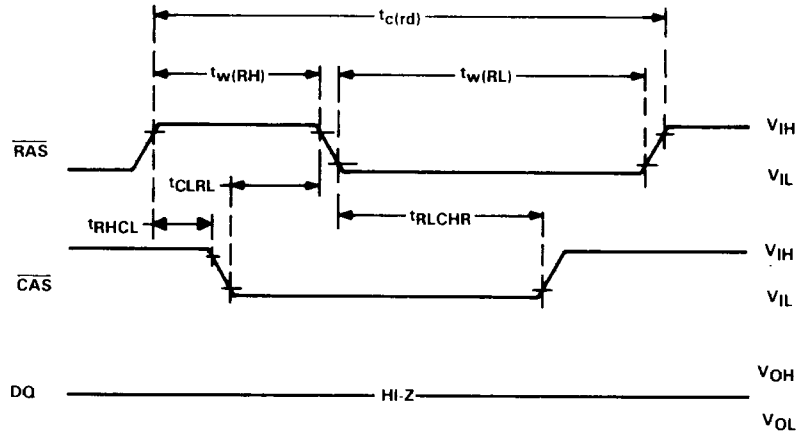
hidden refresh cycle



$\overline{\text{RAS}}$-only refresh cycle timing



$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle timing



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APPLICATIONS LITERATURE AVAILABLE

The following literature is available from Texas Instruments for assistance in DRAM system design. Please contact your local TI sales office to obtain a copy.

Application Reports

- The TMS4464 Topology — In order to effectively test the interaction between individual cells in the TMS4464, it is necessary to have a knowledge of the memory array organization and cell topology. Cell sensitivity can be tested by accessing surrounding cells and monitoring the selected cell for changes in the stored data. (SMBA641)

Technical Paper Reprints

- A 256K DRAM Organized for Applications Solutions — As applications software becomes more sophisticated, the need for high density DRAM will continue to increase. The latest generation of DRAMs, the 256K, will provide four times the amount of memory in the same board area as with 64K DRAMs. In addition, more device features will provide the flexibility to maximize utilization of 256K DRAMs in specific applications. This paper describes a 256K DRAM, its technology and architecture, and how it simplifies the needs of expanding applications. (SMQY001)

Technical Article Reprints

- 256K Dynamic RAM is More Than Just an Upgrade — Silicides, lightly doped drain structures are being tuned for mass production of a next-generation part that improves on the 64K workhorse. (SMQY014)
- Designers Weigh Options for 256K Dynamic-RAM Processes — Hidden-refresh modes make dynamic RAMs look static, while alternate addressing modes vary width of single parts. (5MQY017)

Related Data Sheets

- SMJ4416 Data Sheet — Specifications for the 16K X 4 Dynamic RAM. (SGMS416)
- SMJ4256 Data Sheet — Specifications for the 256K X 1 Dynamic RAM. (SGMS256A)