10-bit successive approximation monolithic A-D converter

ZN432 Series

FEATURES

- Choice of linearity error
- 3 operating temperature ranges
- 20 μs conversion time guaranteed
- Input range as desired
- ±5V supplies, TTL/CMOS compatible
- Parallel and serial outputs
- Bipolar monolithic construction

DESCRIPTION

The ZN432 range of successive approximation analogue to digital converters combine several innovations to provide this function on a fully monolithic silicon integrated circuit. The chip contains a current switching array using a matrix of diffused resistors (no trim required), successive approximation logic with TTL interfacing, 2.5V precision voltage reference with reference amplifier, and fast comparator with good overload recovery. The overall accuracy of the A-D system is sufficient to guarantee no missing codes over the operating temperature range.

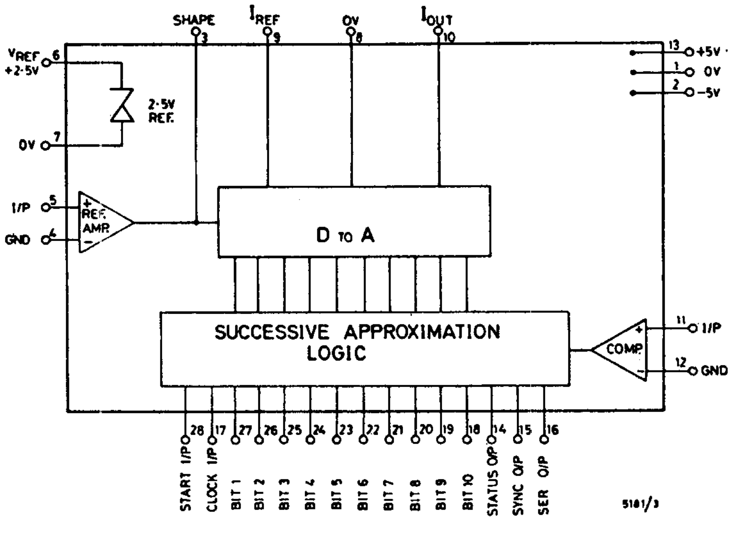


Fig. 1 System diagram

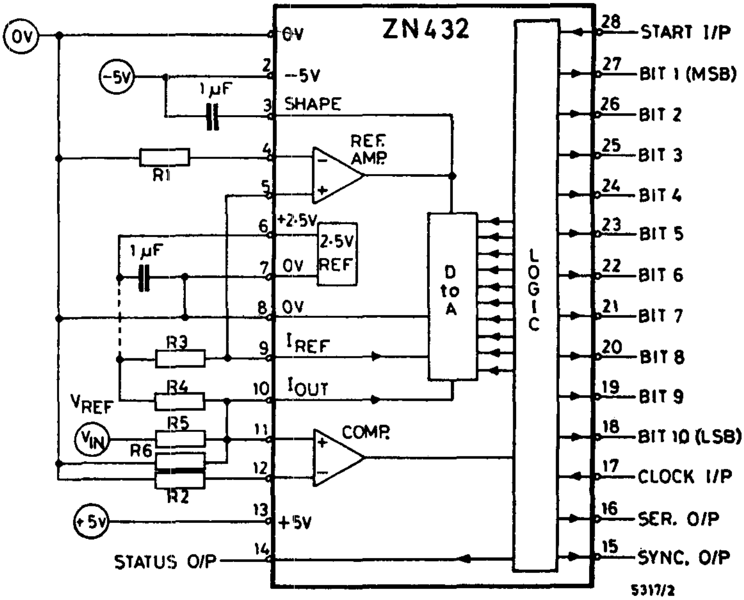


Fig. 2 Typical external components

ORDERING INFORMATION

Device type	Operating temperature	Package
ZN432E	0 to +70°C	Plastic
ZN432J-10	−55 to +125°C	Ceramic
ZN432BJ-10	−40 to +85°C	Ceramic
ZN432CJ-10	0 to 70°C	Ceramic

ABSOLUTE MAXIMUM RATINGS

Supply voltage .. .. ±7V
Logic input voltage .. .. $+V_{CC}$ and 0V
Storage temperature range .. .. −55 to +125°C

CHARACTERISTICS (at ±5V supplies and internal reference unless otherwise specified).

Parameter	Version	t_{amb} = +25°C			Over Spec. Temp. range		Units	Conds.
		Min.	Typ.	Max.	Min.	Max.		
Converter Resolution		10			10		Bits	Note 1
Linearity error	ZN432J-10 ZN432BJ-10 ZN432CJ-10			±0.5		±0.5	LSB	
	ZN432E			±1		±1	LBS	
Differential linearity error	All types		±0.5				LSB	Note 1
DAC reference current, I_{REF}	All types	0.25	0.5	1	0.25	1	mA	Note 2
Conversion time	All types		15	20		20	μs	Note 3
Nominal analogue input range	All types	−2.5		+2.5			V	Note 4
Supply rejection	All types		0.1				%/V	
Gain error	All types		±0.05				%	Note 5
Gain T.C.	ZN432J-10 ZN432BJ-10 ZN432CJ-10		10				ppm/°C	
	ZN432E		20				ppm/°C	
Zero T.C.	ZN432J-10 ZN432BJ-10 ZN432CJ-10		7				ppm/°C	
	ZN432E		15				ppm/°C	
Supply voltage	All types	±4.5	±5	±5.5	±4.5	±5.5	V	
Supply current	All types		35				mA	
Power consumption	All types		350				mW	

CHARACTERISTICS (Cont.)

Parameter	Version	t_{amb} = +25°C Min.	Typ.	Max.	Over Spec. Temp. range Min.	Max.	Units	Conditions
Internal voltage reference								
Output voltage	ZN432J-10, ZN432BJ-10, ZN432CJ-10	2.44	2.48	2.52			V	Note 6
	ZN432E	2.38	2.46	2.54			V	
Slope impedance	All types		0.75				Ω	
Max. load current	All types		±2				mA	
Logic	**All types**							
High level input voltage		2.0			2.0		V	
Low level input voltage				0.8		0.8	V	
High level input current			7				μA	$V_S = \pm 5.5V$, $V_I = 2.4V$
			50				μA	$V_S = \pm 5.5V$, $V_I = 5.5V$
Low level input current			1				μA	$V_S = \pm 5.5V$, $V_I = 0.4V$
High level output voltage		2.4			2.4		V	$I_{load} = -40\mu A$
Low level output voltage				0.4		0.4	V	$I_{load} = 1.6mA$

Note 1 No missing codes over full temperature range at resolution appropriate to accuracy.

Note 2 The full-scale D-A output current $I_{OUT} = 4$ times I_{REF}. For optimum performance $I_{REF} = 0.5mA$.

Note 3 This corresponds to a maximum clock rate of 550kHz based on 11 clock periods per conversion cycle (see timing diagram, page 2-41). This provides an update rate of 45kHz.

Note 4 Single polarity and other input ranges may be provided by different input resistor values. (see page 2-42)

Note 5 Excluding reference

Note 6 For typical temperature performance see Fig. 6, page 2-42.

TEST CIRCUIT

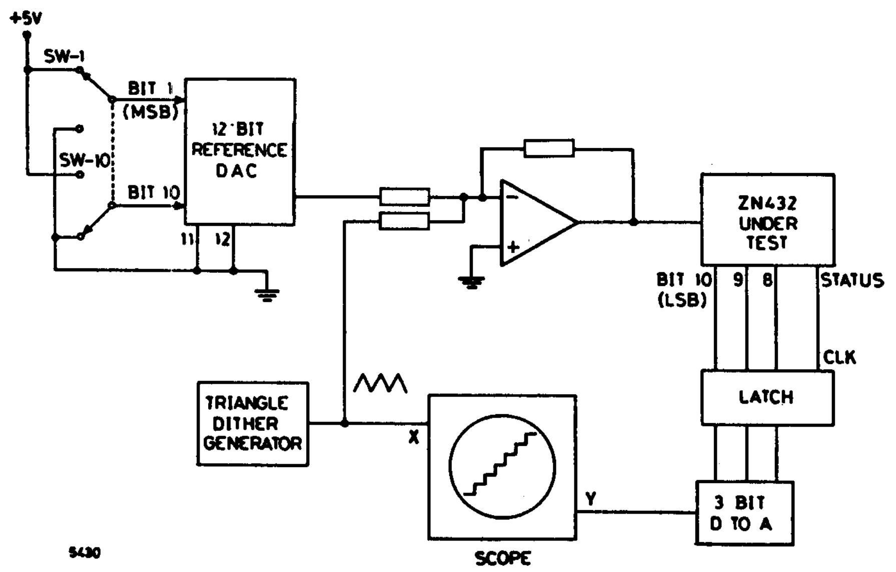


Fig. 3 Dynamic crossplot accuracy test

Switches SW-1 to SW-10 are set to the appropriate digital code to select the point on the characteristic to be displayed. For example, code 10000 00000 would select half full-scale, i.e. the major transition.

The output from the dither generator (suggested peak to peak amplitude = $\pm 4 \times$ LSB) is used as the X deflection for the scope and is also superimposed on the analogue output from the reference DAC in the summing amplifier. The resulting analogue signal including dither is used as V_{IN} for the ZN432 under test.

Bit 10, 9 and 8 outputs are fed to the inputs of a 3-bit DAC of at least 6-bit accuracy and the analogue output used as the Y deflection of the scope. Differential non-linearity is shown by horizontal lines which are longer or shorter than the rest.

CALCULATION OF EXTERNAL RESISTORS (See Fig. 2, page 2-36)

1. R_3, R_4, R_5 can affect gain and offset stability and thus require to be of high quality.
2. R_1 and R_2 are to allow for the bias current of the reference amplifier and comparator, thus:

$$R_1 = R_3$$

And $R_2 =$ parallel combination of R_4, R_5, and R_6.

3. I_{REF} should be 0.5mA

Therefore $$R_3 = \frac{V_{REF}}{0.5mA}$$

I_{outFS} is four times I_{REF}, i.e., 2mA

4. Analysing the network yields the following:

$$R_4 = \frac{-V_{REF}\,R_5}{V_{in}\,min}$$

$$R_5 = \frac{V_{in}\,max - V_{in}\,min}{I_{out\,FS}}$$

Where V_{in} max is the voltage for the logic output to be all 1's.
V_{in} min is the voltage for the logic output to be all 0's.

5. R_6 should be chosen such that the parallel combination of R_4, R_5 and R_6 is about 1.25kΩ as this determines the D-A time constant and hence conversion time.
6. The following is a table of values to give examples of the above equations.

V_{in} max	V_{in} min	V_{REF}	R_1[1]	R_2[1]	R_3	R_4	R_5	R_6[1]
+2.5	−2.5	2.5	5kΩ	1.25kΩ	5kΩ	2.5kΩ	2.5kΩ	∞
+2.5	−2.5	5*	10kΩ	1.25kΩ	10kΩ	5kΩ	2.5kΩ	5kΩ
+2.5	0	2.5	5kΩ	1.25kΩ	5kΩ	∞	1.25kΩ	∞
+5	0	2.5	5kΩ	1.25kΩ	5kΩ	∞	2.5kΩ	2.5kΩ
+4	−2	2.5	5kΩ	1.25kΩ	5kΩ	3.75kΩ	3kΩ	5kΩ
+4	−2	12*	24kΩ	1.25kΩ	24kΩ	3.75kΩ	3kΩ	5kΩ
+10	−10	2.5	5kΩ	1.25kΩ	5kΩ	2.5kΩ	10kΩ	3.33kΩ

Note 1 Nearest prefered value may be used for R_1, R_2 and R_6.

*Note 2 External reference.

7. For setting up R_4 will adjust the offset.
R_3 will adjust the gain.

For unipolar operation where R_4 approaches ∞ and a zero adjustment is required, the following offset circuit is suggested in place of R_4 (Typical values only).

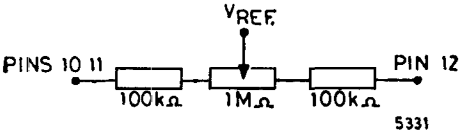


Fig. 4 Offset circuit with unipolar operation

TIMING DETAILS

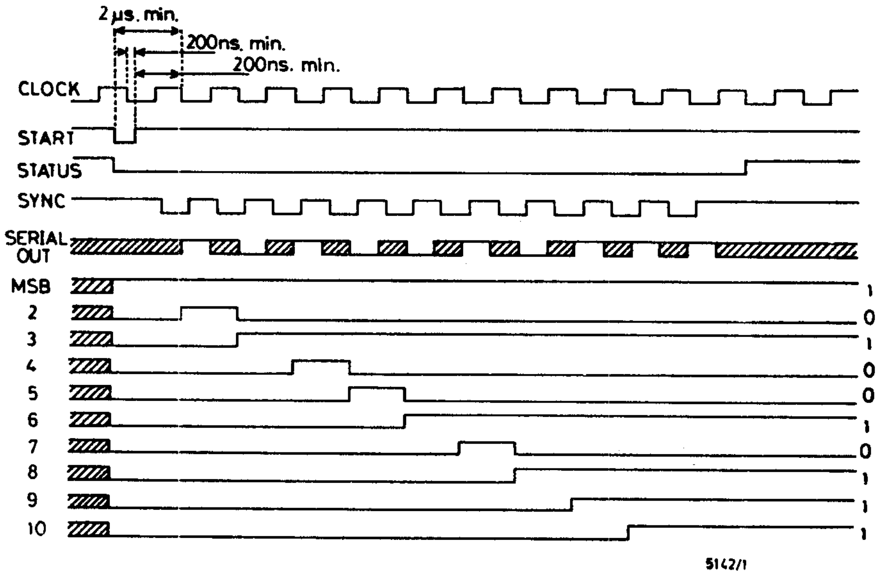


Fig. 5 Timing diagram

NOTES ON TIMING DIAGRAM

1. Conversion is initiated by a 'START' pulse which sets the MSB to 1 and all other bits to 0.

2. The first active (negative going) edge of clock after the trailing edge of the 'START' pulse should not occur until at least 2µs after the leading edge of the 'START' pulse to allow for MSB settling.

3. A negative going edge of clock must not occur within 200ns either side of the trailing edge of the 'START' pulse.

4. As a special case of conditions (2) and (3) the 'START' pulse may be coincident with, and of the same duration as, a negative going clock pulse.

5. Serial data is available during conversion at the Serial Output.

Ten SYNC pulses are provided to facilitate data transmission.

The serial output data is valid on the positive going edge of the SYNC pulse.

6. Cross hatching indicates a 'don't care' condition or, in the case of serial output, invalid data.

7. The conversion sequence shown is for the digital word 1010010111.

8. The parallel output data is valid when the status output goes HIGH.

LOGIC CODING

Table 1 Unipolar operation

Analogue input Notes 1, 2	Digital output code MSB LSB
FS – 1LSB	1111111111
FS – 2LSB	1111111110
¾FS	1100000000
½FS + 1LSB	1000000001
½FS	1000000000
½FS – 1LSB	0111111111
¼FS	0100000000
1LSB	0000000001
0	0000000000

Table 2 Bipolar operation

Analogue input Notes 1, 2	Digital output code MSB LSB
+(FS – 1LSB)	1111111111
+(FS – 2LSB)	1111111110
+(½FS)	1100000000
+(1LSB)	1000000001
0	1000000000
–(1LSB)	0111111111
–(½FS)	0100000000
–(FS – 1LSB)	0000000001
–FS	0000000000

NOTES:

1. Analogue inputs shown are nominal centre values of code.
2. "FS" is full-scale.

OFFSET AND GAIN SETTING

For unipolar, supply an input of ½LSB for transition 0000000000 to 0000000001, and of (full-scale – 1½LSB) for transition 1111111111 to 1111111110.

For bipolar, supply an input of –(full-scale – ½LSB) for transition 0000000000 to 0000000001, and of (full-scale – 1½LSB) for transition 1111111111 to 1111111110.

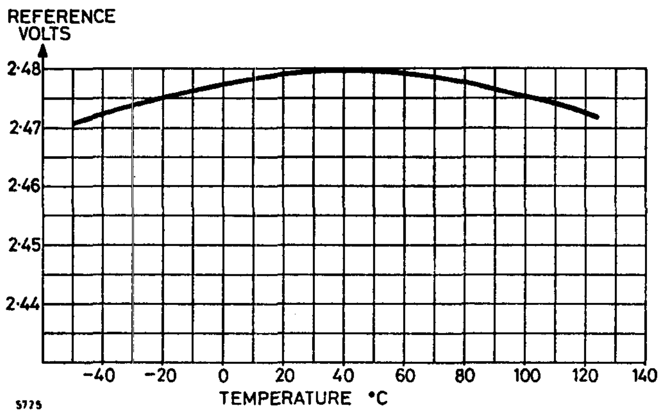
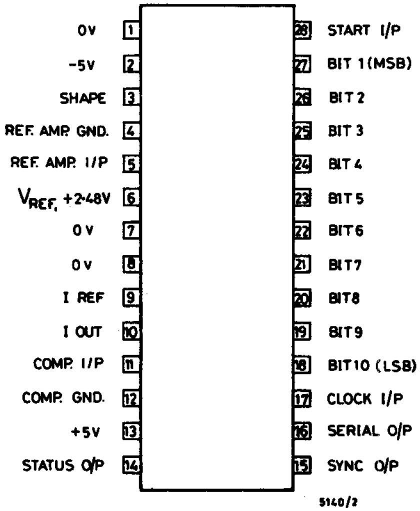
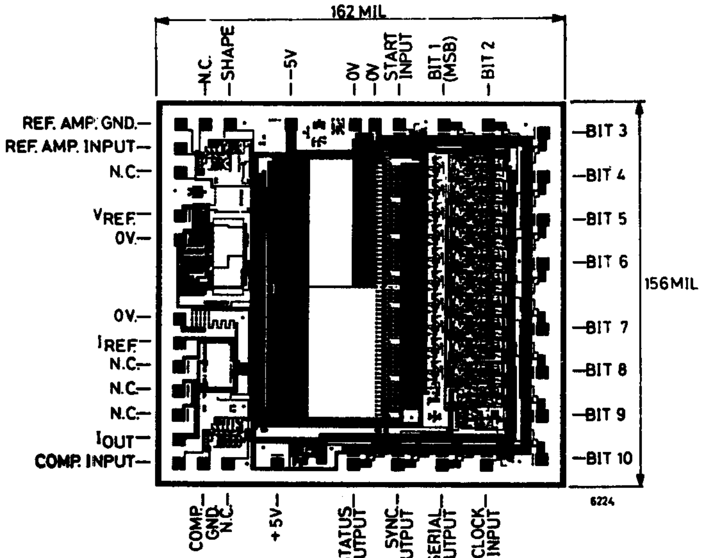


Fig. 6 Typical reference voltage v temperature (all types)

PIN CONNECTIONS





CHIP DIMENSIONS AND LAYOUTS