Der NDR-Klein Computer

Gebrauchs- und Aufbauanleitung

SOUND

Mit der SOUND-Karte des NDR-Klein-Computer lassen sich auf einfache Weise Töne und Geräusche "vom Rechner aus" erzeugen. Das verwandte Spezial-IC enthält 3 unabhängige Tongeratoren, sowie einen Rauschgenerator. Jeder Tongenerator ist sowohl in der Tonhöhe als auch in der Lautstärke programmierbar, beim Rauschgenerator kann die "Tonlage" bestimmt werden.

SCHALTUNGSBESCHREIBUNG

Kernstück der Schaltung, die auf der SOUND-Karte realisiert wurde, ist die Tongenerator-Schaltung AY-3-8912 (IC5). Der 74LS245 (IC1 <Bidirektionaler Bustreiber>), den sie sicherlich von den meisten anderen Karten des NDR-Klein-Computers kennen, verbindet den Tongenerator mit den Datenleitungen des Busses (D0-D7), also mit der CPU des Systems. Ebenfalls wie auf vielen schon bekannten Karten erfolgt die Dekodierung auch hier durch einen 74LS85 (IC4), der über die Busleitungen A4-A7 angesprochen wird. Speziell vom AY-3-8912 benötigte Signale (BDIR, BC1) werden von den Gattern 74LS02 (IC2) und 74LS32 (IC3) erzeugt.

Zusätzlich ist mit IC7 ein kleiner NF-Verstärker auf der SOUND-Karte untergebracht. Die Lautstärke des Verstärkers können Sie mit dem Trimmpotentiometer R4 einstellen. Von diesem NF-Verstärker gelangt das Signal über die Lautsprecherbuchse ST5 direkt an einen kleinen Lautsprecher. Sie können allerdings über die Diodenbuchse ST4 auch an einen externer Verstärker anschließen.

Die Adreßierung

Der AY-3-8912 wird mit 2 Adressen angesprochen. Das Singal B1, das vom 74LS02 (IC2) geliefert wird enthält (auch) eine Adreßinformation. Die untere Adresse, hier E0h, führt an ein internes Adreßregister. Die darin enthaltene Adresse bewirkt die Auswahl von 16 internen Registern. Die Daten werden über die Adresse E1h an den AY-3-8912 gegeben. Über die Adresse E0h können auch Daten aus den internen Registern gelesen werden.

Die Karte wird adreßiert über das Steckfeld ST2.
Hier ist die Belegung:

D	C	B	A	Adressen
offen	offen	offen	offen	F0h, F1h
offen	offen	offen	gesch.	E0h, E1h (*)
offen	offen	gesch.	offen	D0h, D1h
offen	offen	gesch.	gesch	C0h, C1h
offen	gesch.	offen	offen	B0h, B1h
offen	gesch.	offen	gesch.	A0h, A1h
offen	gesch.	gesch.	offen	90h, 91h
offen	gesch.	gesch.	gesch.	80h, 81h
gesch	offen	offen	offen	70h, 71h
:	:	:	:	
gesch.	gesch.	gesch.	gesch.	00h, 01h

(*) Diese Adressen werden vom Grundprogramm MON68K (VS4.3) verwendet.

Die Register des Soundgenerators:

Register	7	6	5	4	3	2	1	0
0: Kanal A Ton LSB:	7	6	5	4	3	2	1	0
1: Kanal A MSB:	x	x	x	x	B	A	9	8
2: Kanal B Ton LSB:	7	6	5	4	3	2	1	0
3: Kanal B MSB:	x	x	x	x	B	A	9	8
4: Kanal C Ton LSB:	7	6	5	4	3	2	1	0
5: Kanal C MSB:	x	x	x	x	B	A	9	8
6: Rauschperiode :	x	x	x	x	3	2	1	0
7: Freigabe 0=an :	I/O IOB	I/O IOA	Rausch C	Rausch B	Rausch A	Ton C	Ton B	Ton A
8: Kanal A Amplit.:	x	x	x	M	L3	L2	L1	L0
9: Kanal B Amplit.:	x	x	x	M	L3	L2	L1	L0
A: Kanal C Amplit.:	x	x	x	M	L3	L2	L1	L0
B: Hällkurven-periode LSB :	7	6	5	4	3	2	1	0
C: Hüllkurven-periode MSB :	F	E	D	C	B	A	9	8
D: Hüllkurvenform :	**x**	**x**	**x**	**x**	Cont.	ATT	ALT	HOLD
E: I/O (Port A) :	7	6	5	4	3	2	1	0

Mit den Registern 0 bis 5 wird die Tonhöhe der einzelnen Generatoren eingestellt. Jeweils zwei Register bestimmen einen Ton. Der Eingangstakt wird durch 16 dividiert, sodann wird durch Herunterzählen eines 12bit-Zählers, der mit dem angegebenen Wert geladen wird, die Ausgangsfrequenz erzeugt.

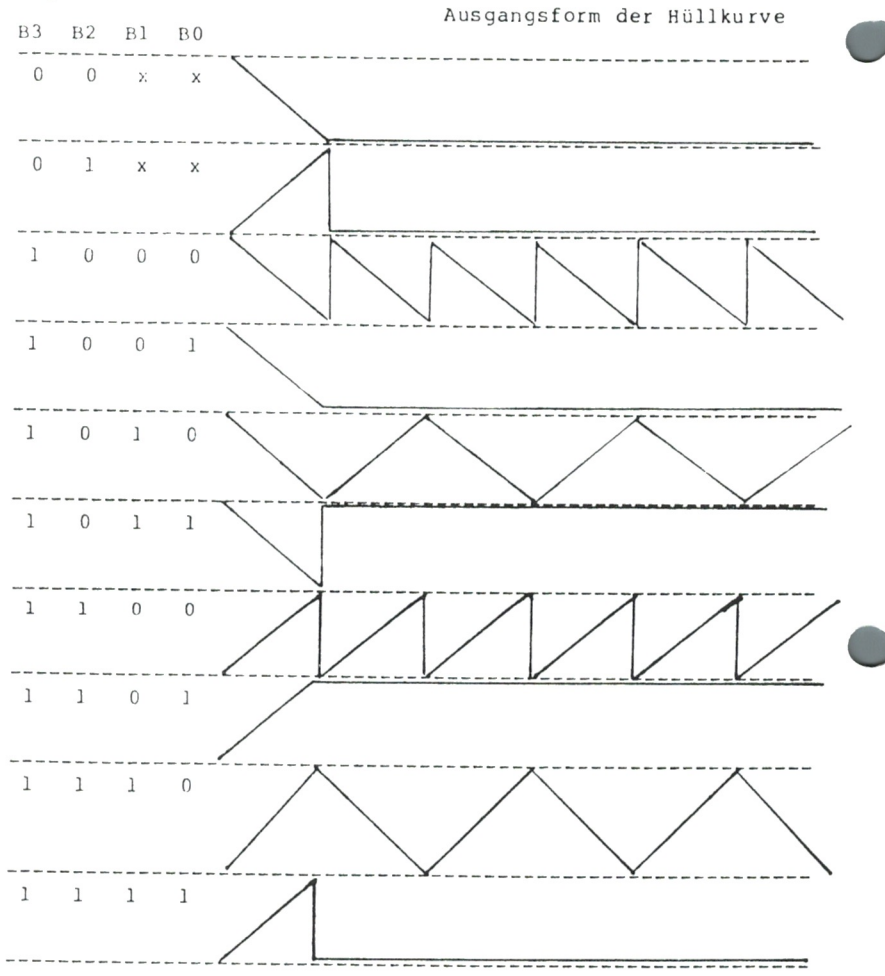
Mit Register 6 wird die Rauschquelle programmiert. Durch Teilen der Taktfrequenz durch 16 wird die Grundfrequenz des Rauschgenerators erreicht. Ein 5bit-Wert lädt dann wieder einen Zähler, der heruntergezählt wird. Damit wird dann die Frequenz des Rauschgenerators eingestellt.

Mit Register 7 können die einzelen Quellen freigegeben werden. Eine 0 gibt sie frei. Über dieses Register wird aber auch der Parallelport im Rauschgenerator-IC freigegeben. Eine 0 definiert hier den Port als Eingang.

Mit den drei Registern 8 bis A kann die Amplitude von Ton oder Rauschen (drei Kanäle) bestimmt werden. Ein Wert von 0 bis 15 gibt die Lautstärke, die logarithmisch eingestellt werden. Soll ein Kanal ausgeschaltet werden, wird der Wert auf 0 gesetzt. Ist Bit4 gesetzt, wird die Lautstärkeneinstellung von einem Hüllkurvengenerator gesteuert. Die Hüllkurvenperiode läßt sich

mit den Registern B und C einstellen, wobei, um auch Perioden von großer Zeitdauer erhalten zu können, mit 16 Bit gearbeitet wird.

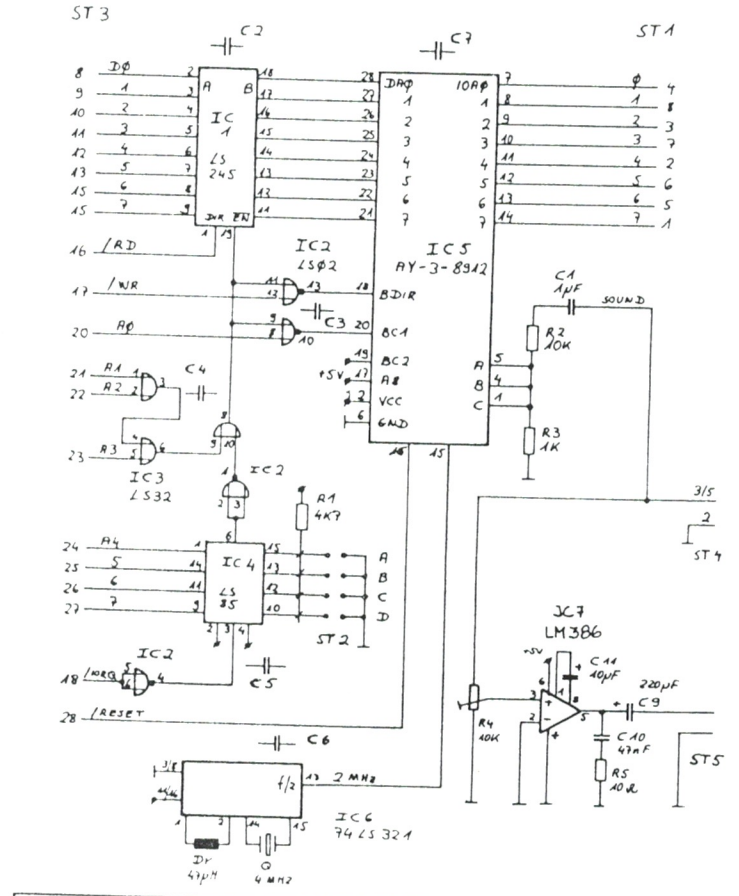
Mit Register D kann die Hüllkurvenform eingestellt werden.



Der Sound-Generator arbeitet mit einer Frequenz von 2MHz. Um diese Frequenz unabhängig vom jeweiligen Prozessortakt zu erhalten, wird sie mit einem Taktoszillator auf der Karte erzeugt.Der Taktoszillator umfaßt die Bauteile Q, IC6, C6, C8 und L1. Der 74LS321 (IC6<Oszillator>) teilt die vom 4MHz-Quarz kommende Frequenz, die dann zum Pin 15 des AY-3-8912 geführt wird.

Auf den Stecker ST1 ist der Parallelport, den der AY-3-8912 beinhaltet herausgeführt. Er kann also von diesem Steckfeld aus verdrahtet werden.

SCHALTUNG

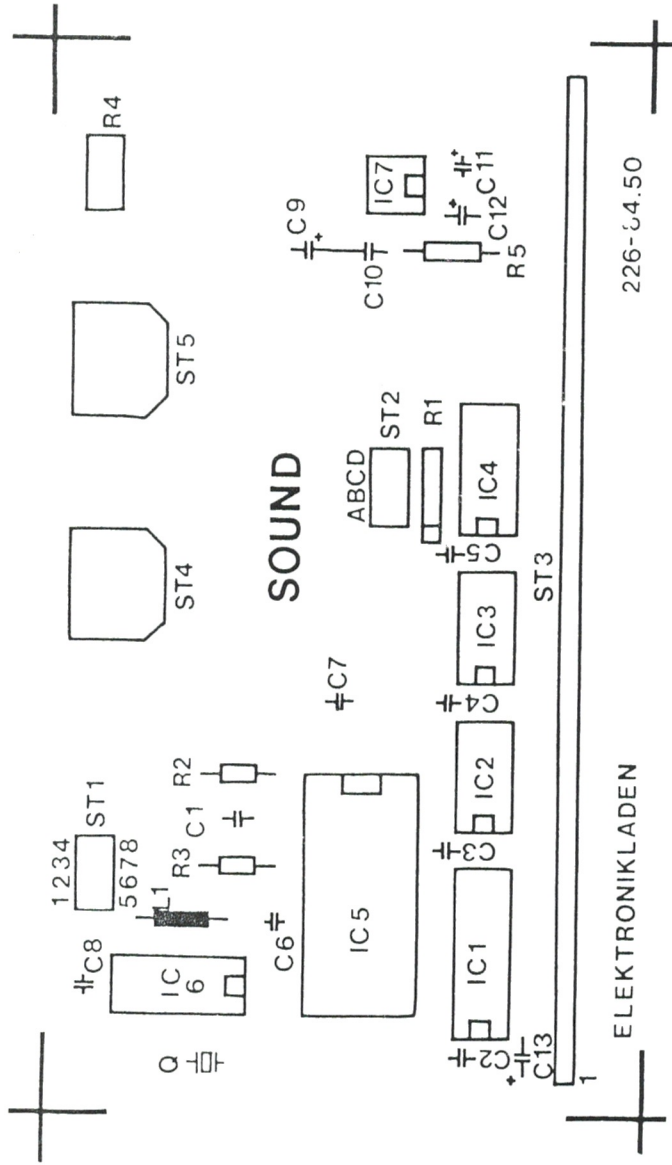


			Maßstab
			SOUND
	84	Datum	Name
	Heute		RBH
	Letzte		
	Nummer		
			Blatt

STÜCKLISTE

Stück	Aufdruck	Beschreibung
1	IC 1	Int. Schaltung 74LS245
1	IC 2	Int. Schaltung 74LS02
1	IC 3	Int. Schaltung 74LS32
1	IC 4	Int. Schaltung 74LS85
1	IC 5	Int. Schaltung AY-3-8912
1	IC 6	Int. Schaltung 74LS321
1	IC 7	Int. Schaltung LM386N-1
1	Q	4MHz Quarz
1	C 1	Folien Kondensator 1uF
7	C 2,3,4,5,6,7,8	Keram. Kondensator 100nF
1	C 9	Elekrolyt Kondens. 220uF/10V
1	C10	Keram. Kondensator 47nF
3	C11,12,13	Tantal Kondensator 10uF/16V
1	L 1	Festinduktivität 47uH
1	R 1	Widerstands Array 4x4,7 KOhm
1	R 2	Widerstand 10KOhm
1	R 3	Widerstand 1Kohm
1	R 4	Trimmpotentiometer 10KOhm
1	R 5	Widerstand 10Ohm
2	ST 1,2	Stiftleiste 2x4pin
1		Stiftleiste abgew. 54pin
1	ST 4	Diodenbuchse 5polig zur Platinenmontage
1	ST 5	Lautsprecherbuchse zur Platinenmontage
1	zu IC 1	IC-Sockel DIL 20
2	zu IC 2,3	IC-Sockel DIL 14
2	zu IC 4,6	IC-Sockel DIL 16
1	zu IC 5	IC-Sockel DIL 28
1	zu IC 7	IC-Sockel DIL 8
4		Jumper
1		Leiterplatte
		Versionsnummer 226-84.50

BESTÜCKUNGSDRUCK



BESTÜCKUNG

Beginnen Sie (wie immer) mit der Bestückung der passiven Bauteile und der Steckerleisten. Achten Sie darauf, daß, wenn Sie die 54polige abgewinkelte Steckerleiste einlöten, alle Pins dieser Leiste parallel zur Leiterplatte stehen. Das gewährleistet, daß die Karte später "gut" in die Buchsen des Busses paßt. Löten Sie nun die Widerstände ein. Winkeln sie die Widerstände am besten vor dem Einlöten ab. Mit einem Seitenschneider sollten Sie nach dem Einlöten die an der Lötseite überstehenden Drähte abschneiden. Vorsicht beim Einlöten des Widerstands Array. Es hat einen gemeinsamen Pol, der auf dem Körper des Netzwerkes mit einem kleinen Punkt (neben der Beschriftung gekennzeichnet.) Im Bestückungsdruck der Karte ist dieser Punkt durch ein kleines Quadrat markiert. Löten Sie nun auch die Festinduktivität L1 ein, die ähnlich wie ein Widerstand aussieht, aber etwas größer ist. Als nächstes kommen die Kondensatoren. Beginnen Sie mit den keramischen Kondensatoren C2 - 8 und C10. Sie wissen, daß keramische Kondensatoren ungepolt sind. Sie müssen hier also nicht auf Plus- oder Minuspol achten, wie bei den Tantal-Kondensatoren C11 - 13, die nun als nächstes eingelötet werden. Auf den Körpern der Kondensatoren finden Sie ein kleines "+"-Zeichen. Auch im Bestückungsdruck finden Sie ein solches Zeichen. Das Beinchen des Kondesators, das dem "+"-Zeichen am nächsten ist, gehört in den auf der Karte mit "+" gekennzeichneten Lötpunkt.Auch der Elektrolykondensator C9 ist gepolt. Bei ihm ist der auf dem Metallkörper der Minuspol gekennzeichnet. Auf der Karte finden Sie den Pluspol markiert. Seien Sie bitte beim Einlöten der gepolten Kondensatoren sehr sorgfältig, denn, wenn Sie an einen falsch gepolten Kondensator Spannung anlegen, kann der sich mit Knall und Stichflamme "verabschieden". Der Folienkondensator C1 ist ungepolt. Bei dem besteht also keine "Explosionsgefahr". Löten Sie als nächstes den Quarz, die IC-Fassungen und beiden Buchsen und das Trimmpotentiometer ein. Wenn Sie die Buchsen und das Potentiometer an der Frontplatte Ihres Rechners unterbringen wolen, verdrahten Sie die Buchsen und das Potentiometer. Beim Trimmpotentiometer finden Sie auch eine kleine Plastikachse. Wenn Sie diese Achse montieren, läßt sich das Poti erheblich leichter einstellen, als mit einem Schraubenzieher. Wenn Sie nun die IC-Fassungen einlöten, achten Sie bitte auf die im Bestückungsdruck angebrachten Markierungen. Sie bezeichnen (wie bei allen Karten) die Lage der integrierten Schaltungen. Auch die IC-Fassungen sind mit einer kleinen Kerbe (Dreieck) entsprechend kennzeichnet. Löten Sie also die Fassungen schon richtig herum ein. Dann haben sie nach dem Einlöten der Fassungen auch keine Schwierigkeiten, die ICs richtig herum einzustecken, denn auf dem Plastikkörper der integrierten Schaltungen finden Sie wiederum eine Kerbe, die sich in der Lage mit den

Markierungen des Bestückungsdruckes und der IC-Fassungen decken soll. Nun sollten Sie, bevor Sie die ICs einsetzen einmal die Versorgungsspannungen messen. Stecken sie die Karte in den Bus und messen Sie: an Pin20 von IC1 müssen ebenso +5V zu messen sein, wie an Pin14 von IC2, Pin14 von IC3, Pin 16 von IC4, Pin3 von IC5, Pin11 und 16 von IC6 und Pin6 von IC7. Wenn das der Fall ist, stecken Sie die ICs nun vorsichtig ein. Winkeln Sie unter Umständen die Beinchen auf einer geraden Fläche etwas an, damit Sie besser in die Fassungen eingeführt werden können. Kontrollieren Sie nun noch einmal die Lage. In der unteren Reihe "schauen" nun alle IC's (IC1,2,3,4) nach links, darüber weist das IC5 nach rechts und IC 6 und 7 nach unten.
Kontrollieren Sie nun (möglichst mit einer Lupe) alle Lötverbindungen, um "kalten" Lötstellen auf die Spur zu kommen. Häufig glänzen "kalte" Lötstellen nicht, sondern wirken, da bei ihnen das Lot nicht "geflossen" ist, matt. Löten Sie verdächtige Lötstellen nach. "Kalte" Lötstellen gehören zu den häufigsten Fehlern und sind oft, wenn sie nicht bei der Sichtkontrolle gefunden werden, oft schlecht zu lokalisieren. Kontrollieren Sie nun (mit der Lupe) auch noch einmal auf der Bestückungsseite, ob alle integrierten Schaltungen richtig stecken. Es kommt vor, daß ein Beinchen eine Bausteins statt in die Fassung zu gleiten, abknickt und nahezu unsichtbar unter dem Plastikkörper des ICs verschwindet.

In Rolf-Dieter Kleins Buch "Mikrocomputer selbstgebaut und programmiert" (2. Auflage) finden Sie auf Seite 201 ein kleines Testprogramm, mit dem sie die Funktion der Schaltung leicht überprüfen können. Auf den Seiten 319 - 323 finden Sie dort auch Listings für einige Beispielprogramme für "Geräuschdemos".

HÄUFIGE FEHLER:

Häufigster bisher aufgetretener Fehler war die falsche Adreßierung der SOUND-Karte. Beachten Sie also genau die Seite 2 dieser Beschreibung.
Außerdem wurde relativ häufig das Widerstandsnetzwerk falsch herum eingelötet und der Elekrolytelko verpolt.

TTL MSI

TYPES SN54LS320, SN54LS321, SN74LS320, SN74LS321 CRYSTAL-CONTROLLED OSCILLATORS

D2418, DECEMBER 1978 – REVISED JANUARY 1981

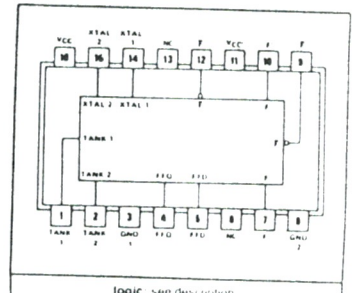
'LS320

- Crystal-Controlled Oscillator Operation from 1 MHz to 20 MHz
- 2-Phase Driver Outputs

'LS321

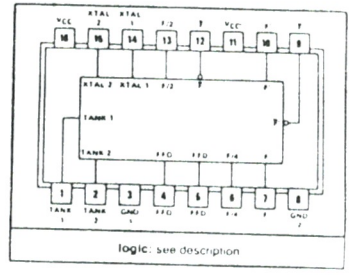
- Similar to 'LS320 But Includes f/2 and f/4 Count-Down Outputs

SN54LS320 . . . J OR W PACKAGE
SN74LS320 . . . J OR N PACKAGE
(TOP VIEW)



NC – No internal connection

SN54LS321 . . . J OR W PACKAGE
SN74LS321 . . . J OR N PACKAGE
(TOP VIEW)



description

The 'LS320 is a crystal-controlled oscillator/clock driver. It features complementary standard and high-current driver outputs. A synchronization flip-flop is included.

The driver outputs, F and $\overline{F}$, have very low impedance and can be used to drive highly capacitive TTL-level lines. If the driver outputs are not used, then the V_{CC}' terminal can be left open.

The 'LS321 is identical to the 'LS320 except it additionally features two count-down outputs, F/2 and F/4.

These circuits were designed for series resonant crystal control of frequency, and capacitative control is not recommended. If a fundamental crystal is used an inductor of 5 to 100 μH with a Q_L of 30 to 40, or a resistor of 130 Ω, is required to be connected between the tank 1 and tank 2 inputs. If a third overtone crystal is used, a tuned tank is necessary. The XTAL 1 and XTAL 2 inputs have an input capacitance of 30 to 32 pF.

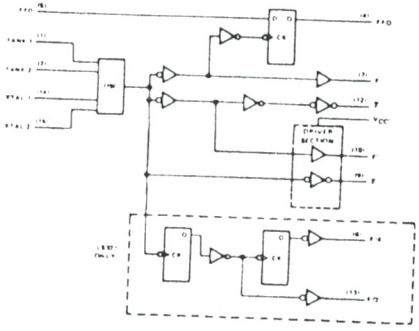
Interaction of the driver outputs with the other outputs limits useful frequencies as shown in the frequency limits table.

The SN54LS320 and SN54LS321 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LS320 and SN74LS321 are characterized for operation from 0°C to 70°C.

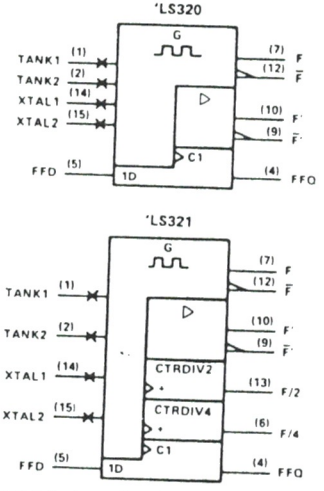
FREQUENCY LIMITS

OUTPUTS IN USE	V_{CC}	V_{CC}'	f_{max}
Driver outputs only	5 V	5 V	20 MHz
Other outputs only	5 V	Open	20 MHz
Driver and any other outputs	5 V	5 V	10 MHz

functional block diagram (positive logic)



logic symbols



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Supply voltage, V_{CC}' . . . . . 7 V
Input voltage to FFD terminal . . . . . −0.5 V to 7 V
Operating free-air temperature range: SN54LS320, SN54LS321 . . . . . −55°C to 125°C
SN74LS320, SN74LS321 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminals.

recommended operating conditions

		SN54LS320 SN54LS321			SN74LS320 SN74LS321			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Supply voltage, V_{CC}'		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	F or F̄			−1.2			−2.4	mA
	F, F̄, F/2, F/4			−0.4			−0.4	
Low-level output current, I_{OL}	F or F̄			12			24	mA
	F, F̄, F/2, F/4			4			8	
Output frequency, f_{out}	F/2 (LS321)	0.5		10	0.5		10	MHz
	F/4 (LS321)	0.25		5	0.25		5	
	F or F̄	1		20	1		20	
Operating free-air temperature, T_A		−55		125	0		70	°C

LM386 low voltage audio power amplifier

general description

The LM386 is a power amplifier designed for use in low voltage consumer applications. The gain is internally set to 20 to keep external part count low, but the addition of an external resistor and capacitor between pins 1 and 8 will increase the gain to any value up to 200.

The inputs are ground referenced while the output is automatically biased to one half the supply voltage. The quiescent power drain is only 24 milliwatts when operating from a 6 volt supply, making the LM386 ideal for battery operation.

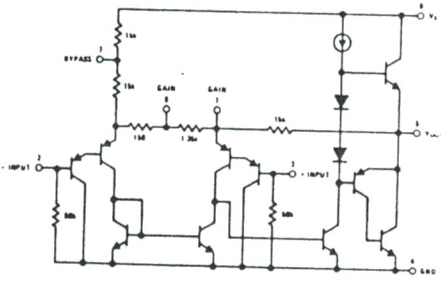
features

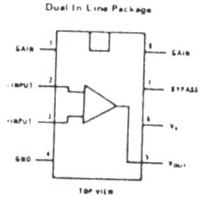
- Battery operation
- Minimum external parts
- Wide supply voltage range — 4V–12V or 5V–18V
- Low quiescent current drain — 4 mA
- Voltage gains from 20 to 200
- Ground referenced input
- Self-centering output quiescent voltage
- Low distortion
- Eight pin dual-in-line package

applications

- AM-FM radio amplifiers
- Portable tape player amplifiers
- Intercoms
- TV sound systems
- Line drivers
- Ultrasonic drivers
- Small servo drivers
- Power converters

equivalent schematic and connection diagrams

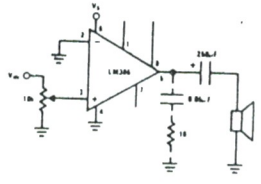




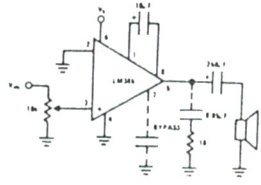
Order Number LM386N-1, LM386N-2, LM386N-3 or LM386N-4
See NS Package N08B

typical applications

Amplifier with Gain = 20
Minimum Parts



Amplifier with Gain = 200



absolute maximum ratings

Supply Voltage (LM386N)	15V	Storage Temperature	−65°C to +150°C
Supply Voltage (LM386N-4)	22V	Operating Temperature	0°C to +70°C
Package Dissipation (Note 1) (LM386A)	1.25W	Junction Temperature	+150°C
Package Dissipation (Note 2) (LM386)	660 mW	Lead Temperature (Soldering, 10 seconds)	+300°C
Input Voltage	±0.4V		

electrical characteristics T_A = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage (V_S)					
LM386		4		12	V
LM386N-4		5		18	V
Quiescent Current (I_Q)	V_S = 6V, V_{IN} = 0		4	8	mA
Output Power (P_{OUT})					
LM386N-1	V_S = 6V, R_L = 8Ω, THD = 10%	250	325		mW
LM386N-2	V_S = 7.5V, R_L = 8Ω, THD = 10%	400	500		mW
LM386N-3	V_S = 9V, R_L = 8Ω, THD = 10%	500	700		mW
LM386N-4	V_S = 16V, R_L = 32Ω, THD = 10%	700	1000		mW
Voltage Gain (A_V)	V_S = 6V, f = 1 kHz		26		dB
	10μF from Pin 1 to 8		46		dB
Bandwidth (BW)	V_S = 6V, Pins 1 and 8 Open		300		kHz
Total Harmonic Distortion (THD)	V_S = 6V, R_L = 8Ω, P_{OUT} = 125 mW f = 1 kHz, Pins 1 and 8 Open		0.2		%
Power Supply Rejection Ratio (PSRR)	V_S = 6V, f = 1 kHz, C_{BYPASS} = 10μF Pins 1 and 8 Open, Referred to Output		50		dB
Input Resistance (R_{IN})			50		kΩ
Input Bias Current (I_{BIAS})	V_S = 6V, Pins 2 and 3 Open		250		nA

Note 1 For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 100°C/W junction to ambient.

Note 2 For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 181°C/W junction to ambient.

application hints

GAIN CONTROL

To make the LM386 a more versatile amplifier, two pins (1 and 8) are provided for gain control. With pins 1 and 8 open the 1.35 kΩ resistor sets the gain at 20 (26 dB). If a capacitor is put from pin 1 to 8, bypassing the 1.35 kΩ resistor, the gain will go up to 200 (46 dB). If a resistor is placed in series with the capacitor, the gain can be set to any value from 20 to 200. Gain control can also be done by capacitively coupling a resistor (or FET) from pin 1 to ground.

Additional external components can be placed in parallel with the internal feedback resistors to tailor the gain and frequency response for individual applications. For example, we can compensate poor speaker bass response by frequency shaping the feedback path. This is done with a series RC from pin 1 to 5 (paralleling the internal 15kΩ resistor). For 6 dB effective bass boost: R ≥ 15 kΩ, the lowest value for good stable operation is R = 10 kΩ if pin 8 is open. If pins 1 and 8 are bypassed then R as low as 2 kΩ can be used. This restriction is because the amplifier is only compensated for closed loop gains greater than 9.

INPUT BIASING

The schematic shows that both inputs are biased to ground with a 50 kΩ resistor. The base current of the input transistors is about 250 nA, so the inputs are at about 12.5 mV when left open. If the dc source resistance driving the LM386 is higher than 250 kΩ it will contribute very little additional offset (about 2.5 mV at the input, 50 mV at the output). If the dc source resistance is less than 10 kΩ, then shorting the unused input to ground will keep the offset low (about 2.5 mV at the input, 50 mV at the output). For dc source resistances between these values we can eliminate excess offset by putting a resistor from the unused input to ground, equal in value to the dc source resistance. Of course all offset problems are eliminated if the input is capacitively coupled.

When using the LM386 with higher gains (bypassing the 1.35 kΩ resistor between pins 1 and 8) it is necessary to bypass the unused input, preventing degradation of gain and possible instabilities. This is done with a 0.1μF capacitor or a short to ground depending on the dc source resistance on the driven input.

GENERAL INSTRUMENT

AY-3-8910 AY-3-8912
AY-3-8913

Programmable Sound Generator

FEATURES

- Full Software Control of Sound Generation
- Interfaces to Most 8-Bit and 16-Bit Microprocessors
- Three Independently Programmed Analog Outputs
- Two 8-Bit General Purpose I/O Ports (AY-3-8910)
- One 8-Bit General Purpose I/O Port (AY-3-8912)
- Single +5 Volt Supply

DESCRIPTION

The AY-3-8910/8912/8913 Programmable Sound Generator (PSG) is a LSI Circuit which can produce a wide variety of complex sounds under software control. The AY-3-8910/8912/8913 is manufactured in the General Instrument N-Channel Ion Implant Process. Operation requires a single +5V power supply, a TTL compatible clock, and a microprocessor controller such as the General Instrument 16-bit CP1610 or one of the PIC1650 series of 8-bit microcomputers.

The PSG is easily interfaced to any bus oriented system. Its flexibility makes it useful in applications such as music synthesis, sound effects generation, audible alarms, tone signalling and FSK modems. The analog sound outputs can each provide 4 bits of logarithmic digital to analog conversion, greatly enhancing the dynamic range of the sounds produced.

In order to perform sound effects while allowing the processor to continue its other tasks, the PSG can continue to produce sound after the initial commands have been given by the control processor. The fact that realistic sound production often involves more than one effect is satisfied by the three independently controllable channels available in the PSG.

All of the circuit control signals are digital in nature and intended to be provided directly by a microprocessor/microcomputer. This means that one PSG can produce the full range of required sounds with no change in external circuitry. Since the frequency response of the PSG ranges from sub-audible at its lowest frequency to post-audible at its highest frequency, there are few sounds which are beyond reproduction with only the simplest electrical connections.

Since most applications of a microprocessor PSG system would also require interfacing between the outside world and the microprocessor, this facility has been designed into the PSG. The AY-3-8910 has two general purpose 8-bit I/O ports and is supplied in a 40 lead package, the AY-3-8912 has one port and 28 leads, the AY-3-8913 has no ports and 24 leads.

PIN FUNCTIONS

DA7--DA0 (input/output/high impedance) pins 30--37 (AY-3-8910)
Data/Address 7--0: pins 21--28 (AY-3-8912)
pins 4--11 (AY-3-8913)

These 8 lines comprise the 8-bit bidirectional bus used by the microprocessor to send both data and addresses to the PSG and to receive data from the PSG. In the data mode, DA7--DA0 correspond to Register Array bits B7--B0. In the address mode, DA3--DA0 select the register number ($0--17_8$) and a DA7--DA4 in conjunction with address inputs $\overline{A9}$ and A8 for the high order address (chip select).

A8 (input): pin 25 (AY-3-8910)
pin 17 (AY-3-8912)
pin 23 (AY-3-8913)

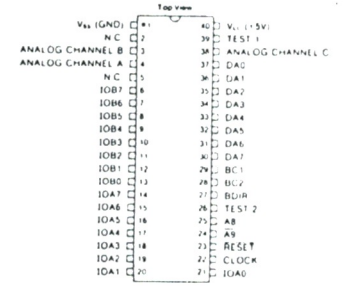
$\overline{A9}$ (input): pin 24 (AY-3-8910)
pin 22 (AY-3-8913)
(not provided on AY-3-8912)

Address 9, Address 8

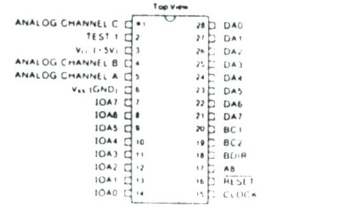
These "extra" address bits are made available to enable the positioning of the PSG (assigning a 16 word memory space) in a total 1,024 word memory area rather than in a 256 word memory area as defined by address bits DA7--DA0 alone. If the memory size does not require the use of these extra address lines they may be left unconnected as each is provided with either an on-chip pull down ($\overline{A9}$) or pull-up (A8) resistor. In "noisy" environments, however, it is recommended that A9 and A8 be tied to an external ground and +5V respectively if they are not to be used.

PIN CONFIGURATIONS

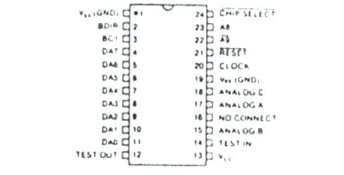
40 LEAD DUAL IN LINE
AY-3-8910



28 LEAD DUAL IN LINE
AY-3-8912



24 LEAD DUAL IN LINE



RESET (input) pin 23 (AY-3-8910) pin 21 (AY-3-8913)
pin 16 (AY-3-8912)

For initialization power-on purposes, applying a logic '0' (ground) to the Reset pin will reset all registers to '0'. The Reset pin is provided with an on-chip pull-up resistor.

CLOCK (input) pin 22 (AY-3-8910) pin 20 (AY-3-8913)
pin 15 (AY-3-8912)

This TTL-compatible input supplies the timing reference for the Tone, Noise and Envelope Generators.

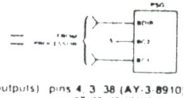
BDIR, BC2, BC1 (inputs) pins 27,28,29 (AY-3-8910)
pins 18,19,20 (AY-3-8912) pins 2, 3 (No BC2 on AY-3-8913
Bus DIRection, Bus Control 2,1 see below)

These bus control signals are generated directly by the CP1610 series of microprocessors to control all external and internal bus operations in the PSG. When using a processor other than the CP1610, these signals can be provided either by comparable bus signals or by simulating the signals on I/O lines of the processor. The PSG decodes these signals as illustrated in the following:

BDIR	BC2	BC1	CP1610 FUNCTION	PSG FUNCTION
0	0	0	NACT	INACTIVE See 010 (DAB)
0	0	1	ADAR	LATCH ADDRESS See 111 (INTAK)
0	1	0	DAB	INACTIVE The PSG/CPU bus is inactive. DA7—DA0 are in a high impedance state
0	1	1	DTB	READ FROM PSG. This signal causes the contents of the register, which is currently addressed, to appear on the PSG/CPU bus. DA7--DA0 are in the output mode
1	0	0	BAR	LATCH ADDRESS. See 111 (INTAK)
1	0	1	DW	INACTIVE See 010 (DAB)
1	1	0	DWS	WRITE TO PSG. This signal indicates that the bus contains register data which should be latched into the currently addressed register. DA7--DA0 are in the input mode
1	1	1	INTAK	LATCH ADDRESS. This signal indicates that the bus contains a register address which should be latched in the PSG. DA7--DA0 are in the input mode

While interfacing to a processor other than the CP1610 would simply require simulating the above decoding, the redundancies in the PSG functions vs. bus control signals can be used to advantage in that only four of the eight possible decoded bus functions are required by the PSG. This could simplify the programming of the bus control signals to the following, which would only require that the processor generate two bus control signals (BDIR and BC1, with BC2 tied to +5V). This is the case with the AY-3-8913 with BC2 pulled high internally.

BDIR	BC1	PSG FUNCTION
0	0	INACTIVE
0	1	READ FROM PSG
1	0	WRITE TO PSG
1	1	LATCH ADDRESS



ANALOG CHANNEL A, B, C (outputs) pins 4, 3, 38 (AY-3-8910)
pins 5, 4, 1 (AY-3-8912) pins 17, 15, 18 (AY-3-8913)

Each of these signals is the output of its corresponding D/A Converter and provides an up to 1V peak-peak signal representing the complex sound waveshape generated by the PSG.

IOA7--IOA0 (input/output) pins 14 - 21 (AY-3-8910)
pins 7 - 14 (AY-3-8912) (not provided on AY-3-8913)

IOB7--IOB0 (input/output) pins 6 - 13 (AY-3-8910)
(not provided on AY-3-8912) (not provided on AY-3-8913)

Input/Output A7--A0, B7--B0

Each of these two parallel input/output ports provides 8 bits of parallel data to from the PSG CPU bus from to any external devices connected to the IOA or IOB pins. Each pin is provided with an on-chip pull-up resistor, so that when in the 'input' mode all pins will read normally high. Therefore, the recommended method for scanning external switches would be to ground the input bit.

TEST 1: pin 39 (AY-3-8910) pin 14 (AY-3-8913) pin 2 (AY-3-8912)
TEST 2: pin 26 (AY-3-8910) pin 12 (AY-3-8913)
(not connected on AY-3-8912)

These pins are for General Instrument test purposes only and should be left open - do not use as tie-points.

V_{CC}: pin 40 (AY-3-8910) pin 13 (AY-3-8913) pin 3 (AY-3-8912)
Nominal +5Volt power supply to the PSG.

V_{SS}: pin 1 (AY-3-8910) pin 19 (AY-3-8913) pin 6 (AY-3-8912)
Ground reference for the PSG.

CHIP SELECT (input) Pin 24 (AY-3-8913 only)
This input signal goes low to enable the PSG to read data on the data bus or write data from the data bus to one of the internal registers. For these above operations to occur, this signal must be true in addition to the current bus address being a valid PSG address. This signal must be valid for all read and write operations. The pin has an internal pull down to V_{SS}.

ARCHITECTURE

The AY-3-8910/8912/8913 is a register oriented Programmable Sound Generator (PSG). Communication between the processor and the PSG is based on the concept of memory-mapped I/O. Control commands are issued to the PSG by writing to 16 memory-mapped registers. Each of the 16 registers within the PSG is also readable so that the microprocessor can determine, as necessary, present states or stored data values.

All functions of the PSG are controlled through the 16 registers which once programmed, generate and sustain the sounds, thus freeing the system processor for other tasks.

REGISTER ARRAY

The principal element of the PSG is the array of 16 read/write control registers. These 16 registers look to the CPU as a block of memory and as such occupy a 16 word block out of 1,024 possible addresses. The 10 address bits (8 bits on the common data/address bus, and 2 separate address bits A8 and $\overline{A9}$) are decoded as follows:

* $\overline{A9}$	A8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
0	1	0	0	0	0	0	0	0	0
THRU									
0	1	0	0	0	0	1	1	1	1
HIGH ORDER (Chip Select)						LOW ORDER (Register No.)			

* $\overline{A9}$ is not provided on the AY-3-8912

The four low order address bits select one of the 16 registers (R0--$R17_8$). The six high order address bits function as 'chip selects' to control the tri-state bidirectional buffers (when the high order address bits are 'incorrect', the bidirectional buffers are forced to a high impedance state). High order address bits $\overline{A9}$, A8 are fixed in the PSG design to recognize a 01 code; high order address bits DA7--DA4 may be mask-programmed to any 4-bit code by a special order factory mask modification. Unless otherwise specified, address bits DA7--DA4 are programmed to recognize only a 0000 code. A valid high order address latches the register address (the low order 4 bits) in the Register Address Latch/Decoder block. A latched address will remain valid until the receipt of a new address, enabling multiple reads and writes of the same register contents without the need for redundant re-addressing.

Conditioning of the Register Address Latch/Decoder and the Bidirectional Buffers to recognize the bus function required (inactive, latch address, write data, or read data) is accomplished by the Bus Control Decode block.

SOUND GENERATING BLOCKS

The basic blocks in the PSG which produce the programmed sounds include:

Tone Generators	produce the basic square wave tone frequencies for each channel (A,B,C)
Noise Generator	produces a frequency modulated pseudo random pulse width square wave output
Mixers	combine the outputs of the Tone Generators and the Noise Generator. One for each channel (A,B,C)
Amplitude Control	provides the D/A Converters with either a fixed or variable amplitude pattern. The fixed amplitude is under direct CPU control; the variable amplitude is accomplished by using the output of the Envelope Generator
Envelope Generator	produces an envelope pattern which can be used to amplitude modulate the output of each Mixer
D/A Converters	the three D/A Converters each produce up to a 16 level output signal as determined by the Amplitude Control

I/O PORTS

Two additional blocks are shown in the PSG Block Diagram which have nothing directly to do with the production of sound -- these are the two I/O Ports (A and B). Since virtually all uses of microprocessor based sound would require interfacing between the outside world and the processor, this facility has been included in the PSG. Data to/from the CPU bus may be read/written to either of two 8-bit I/O Ports without affecting any other function of the PSG. The I/O Ports are TTL-compatible and are provided with internal pull-ups on each pin. Both Ports are available on the AY-3-8910; only I/O Port A is available on the AY-3-8912; no ports are available on the AY-3-8913.

PSG BLOCK DIAGRAM

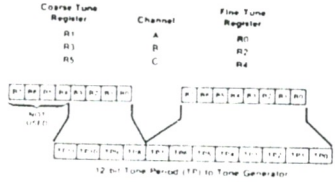
OPERATION

Since all functions of the PSG are controlled by the processor via a series of register loads, a detailed description of the PSG operation can best be accomplished by relating each PSG function to the control of its corresponding register. The function of creating or programming a specific sound or sound effect logically follows the control sequence listed.

Operation	Registers	Function
Tone Generator Control	R0–R5	Program tone periods
Noise Generator Control	R6	Program noise period
Mixer Control	R7	Enable tone and or noise on selected channels
Amplitude Control	R10–R12	Select fixed or envelope variable amplitudes
Envelope Generator Control	R13–R15	Program envelope period and select envelope pattern

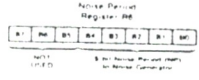
Tone Generator Control (Registers R0, R1, R2, R3, R4, R5)

The frequency of each square wave generated by the three Tone Generators (one each for Channels A, B, and C) is obtained in the PSG by first counting down the input clock by 16, then by further counting down the result by the programmed 12-bit Tone Period value. Each 12-bit value is obtained in the PSG by combining the contents of the relative Coarse and Fine Tune registers, as illustrated in the following.



Noise Generator Control (Register R6)

The frequency of the noise source is obtained in the PSG by first counting down the input clock by 16, then by further counting down the result by the programmed 5-bit Noise Period value. This 5-bit value consists of the lower 5 bits (B4–B0) of register R6, as illustrated in the following.



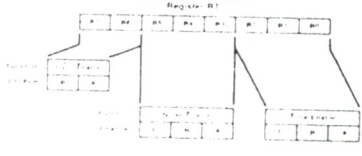
Mixer Control-I/O Enable (Register R7)

Register R7 is a multi-function Enable register which controls the three Noise-Tone Mixers and the two general purpose I/O Ports.

The Mixers, as previously described, combine the noise and tone frequencies, for each of the three channels. The determination of combining neither, either, both noise and tone frequencies on each channel is made by the state of bits B5, B0 of R7.

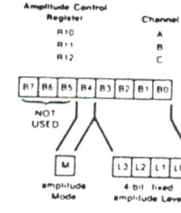
The direction (input or output) of the two general purpose I/O Ports (IOA and IOB) is determined by the state of bits B7 and B6 of R7.

These functions are illustrated in the following.



Amplitude Control (Registers R10, R11, R12)

The amplitudes of the signals generated by each of the three D/A Converters (one each for Channels A, B and C) is determined by the contents of the lower 5 bits (B4–B0) of registers R10, R11, and R12 as illustrated in the following.

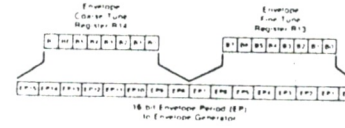


Envelope Generator Control (Registers R13, R14, R15)

To accomplish the generation of fairly complex envelope patterns, two independent methods of control are provided in the PSG: first, it is possible to vary the frequency of the envelope using registers R13 and R14; and second, the relative shape and cycle pattern of the envelope can be varied using register R15. The following paragraphs explain the details of the envelope control functions, describing first the envelope period control and then the envelope shape/cycle control.

ENVELOPE PERIOD CONTROL (Registers R13, R14)

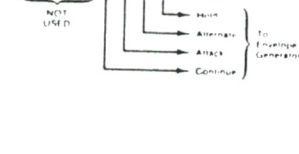
The frequency of the envelope is obtained in the PSG by first counting down the input clock by 256, then by further counting down the result by the programmed 16-bit Envelope Period value. This 16-bit value is obtained in the PSG by combining the contents of the Envelope Coarse and Fine Tune registers, as illustrated in the following.



ENVELOPE SHAPE/CYCLE CONTROL (Register R15)

The Envelope Generator further counts down the envelope frequency by 16, producing a 16-state per cycle envelope pattern as defined by its 4-bit counter output E3,E2,E1,E0. The particular shape and cycle pattern of any desired envelope is accomplished by controlling the count pattern (count up/count down) of the 4-bit counter and by defining a single-cycle or repeat-cycle pattern.

This envelope shape/cycle control is contained in the lower 4 bits (B3–B0) of register R15. Each of these 4 bits controls a function in the envelope generator, as illustrated in the following.



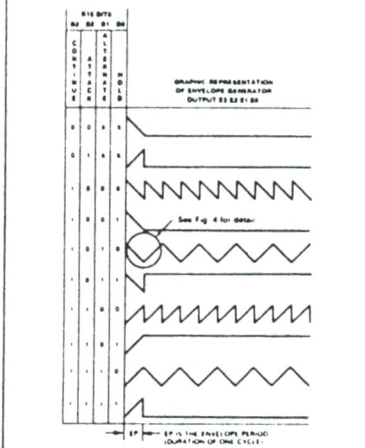


Fig. 1 ENVELOPE SHAPE/CYCLE OPERATION

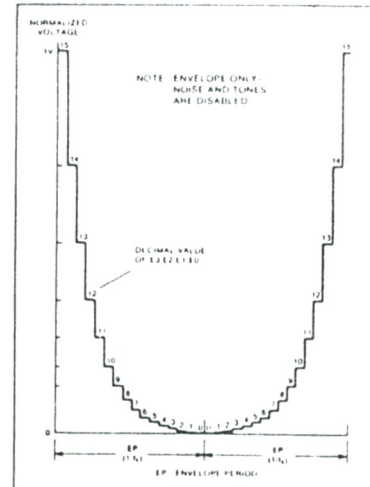


Fig. 3 D/A CONVERTER OUTPUT

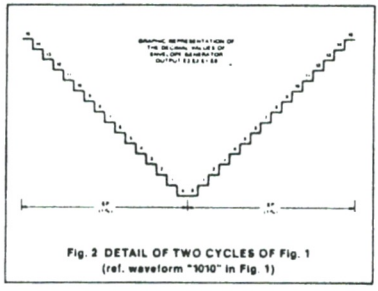


Fig. 2 DETAIL OF TWO CYCLES OF Fig. 1
(ref. waveform "1010" in Fig. 1)

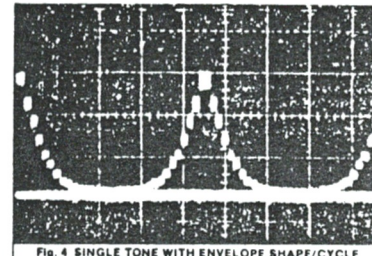


Fig. 4 SINGLE TONE WITH ENVELOPE SHAPE/CYCLE PATTERN 1010

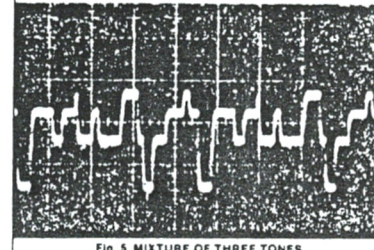


Fig. 5 MIXTURE OF THREE TONES WITH FIXED AMPLITUDES

I/O Port Data Store
(Registers R16, R17)

Registers R16 and R17 function as intermediate data storage registers between the PSG/CPU data bus (DA0--DA7) and the two I/O ports (IOA7--IOA0 and IOB7--IOB0). Both ports are available in the AY-3-8910 only. I/O Port A is available in the AY-3-8912; none are available on the AY-3-8913. Using registers R16 and R17 for the transfer of I/O data has no effect on sound generation.

D/A Converter Operation

Since the primary use of the PSG is to produce sound for the highly imperfect amplitude detection mechanism of the human ear, the D/A conversion is performed in logarithmic steps with a normalized voltage range of from 0 to 1 Volt. The specific amplitude control of each of the three D/A Converters is accomplished by the three sets of 4-bit outputs of the Amplitude Control block, while the Mixer outputs provide the base signal frequency (Noise and/or Tone).

ELECTRICAL CHARACTERISTICS (AY-3-8910, AY-3-8912)

Maximum Ratings*

Storage Temperature ..... −55°C to +150°C
Operating Temperature ..... 0°C to +40°C
V_{CC} and all other Input/Output Voltages with Respect to V_{SS} ..... −0.3V to +8.0V

Standard Conditions (unless otherwise noted)

V_{CC} = +5V ±5%
V_{SS} = GND
Operating Temperature = 0°C to +40°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Characteristics	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
All Inputs						
Low Level	V_{IL}	0	—	0.8	V	
High Level	V_{IH}	2.4	—	V_{CC}	V	
All Outputs (except Analog Channel Outputs)						
Low Level	V_{OL}	0	—	0.5	V	I_{OL} = 1.6mA, 20pf
High Level	V_{OH}	2.4	—	V_{CC}	V	I_{OH} = 100μA, 20pf
Analog Channel Outputs	V_o	0	—	60	dB	Test Circuit Fig. 6
Power Supply Current	I_{CC}	—	45	85	mA	
AC CHARACTERISTICS						
Clock Input						
Frequency	f_C	1	—	2	MHz	Fig. 7
Rise Time	t_r	—	—	50	ns	
Fall Time	t_f	—	—	50	ns	
Duty Cycle	—	25	50	85	%	
Bus Signals (BDIR, BC2, BC1)						
Associative Delay Time	t_{AD}	—	—	50	ns	
Reset						
Reset Pulse Width	t_{RW}	500	—	—	ns	Fig. 8
Reset to Bus Control Delay Time	t_{RB}	100	—	—	ns	
A9, A8, DA7--DA0 (Address Mode)						
Address Setup Time	t_{AS}	400	—	—	ns	Fig. 9
Address Hold Time	t_{AH}	100	—	—	ns	
DA7--DA0 (Write Mode)						
Write Data Pulse Width	t_{DW}	500	—	10 000	ns	Fig. 10
Write Data Setup Time	t_{DS}	50	—	—	ns	
Write Data Hold Time	t_{DH}	100	—	—	ns	
DA7--DA0 (Read Mode)						
Read Data Access Time	t_{DA}	—	250	500	ns	Fig. 11
DA7--DA0 (Inactive Mode)						
Tristate Delay Time	t_{TS}	—	100	200	ns	

**Typical values are at +25°C and nominal voltages

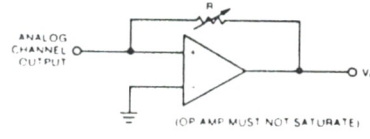


Fig. 6 ANALOG CHANNEL OUTPUT TEST CIRCUIT

ELECTRICAL CHARACTERISTICS (AY-3-8913)

Maximum Ratings*

Storage Temperature ..... −55°C to +150°C
Operating Temperature ..... 0°C to +70°C
V_{CC} and all other Input/Output Voltages with Respect to V_{SS} ..... −0.3V to +8.0V

Standard Conditions (unless otherwise noted):

V_{CC} = +5V ±5%
V_{SS} = GND
Operating Temperature = 0°C to +70°C

* Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Characteristics	Sym	Min	Max	Units	Conditions
DC CHARACTERISTICS					
Input Voltage Levels					
Low Level	V_{IL}	0	0.7	V	
High Level	V_{IH}	2.2	V_{CC}	V	
Output Voltage Levels (except Analog Channel Outputs)					
Low Level	V_{OL}	0	0.4	V	1 TTL Load
High Level	V_{OH}	2.4	V_{CC}	V	+100pf
Analog Channel Outputs	V_O	0	2000	μA	Test Circuit Fig. 6
Power Supply Current	I_{CC}	—	85	mA	
AC CHARACTERISTICS					
Clock Input					
Frequency	f_c	1	2.5	MHz	Fig. 7
Rise Time	t_r	—	50	ns	
Fall Time	t_f	—	50	ns	
Duty Cycle	—	40	60	%	
Bus Signals (BDIR, BC2, BC1)					
Associative Delay Time	t_{BD}	—	50	ns	
Reset					
Reset Pulse Width	t_{RW}	5	—	μs	Fig. 8
Reset to Bus Control Delay Time	t_{RB}	100	—	ns	
A9, A8, DA7—DA0 (Address Mode)					
Address Setup Time	t_{AS}	300	—	ns	Fig. 9
Address Hold Time	t_{AH}	50	—	ns	
DA7—DA0 (Write Mode)					
Write Data Pulse Width	t_{DW}	1800	—	ns	Fig. 10
Write Data Setup Time	t_{DS}	50	—	ns	
Write Data Hold Time	t_{DH}	100	—	ns	
DA7—DA0 (Read Mode)					
Read Data Access Time	t_{DA}	—	350	ns	Fig. 11
DA7—DA0 (Inactive Mode)					
Tristate Delay Time	t_{TS}	—	400	ns	

TIMING DIAGRAMS

Fig. 7 CLOCK AND BUS SIGNAL TIMING

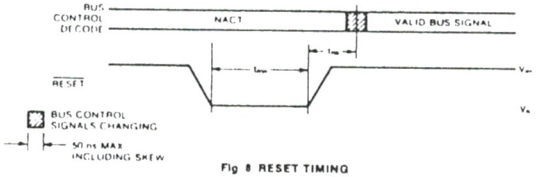


Fig. 8 RESET TIMING

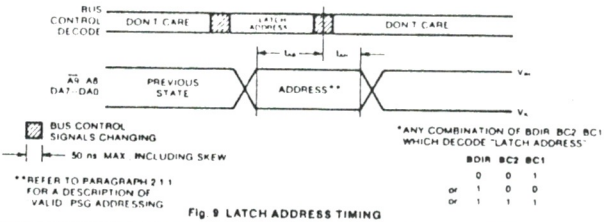


Fig. 9 LATCH ADDRESS TIMING

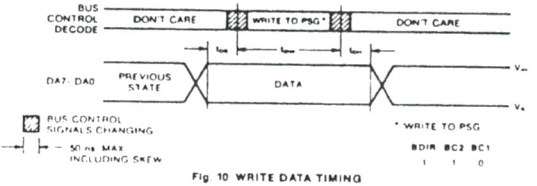


Fig. 10 WRITE DATA TIMING

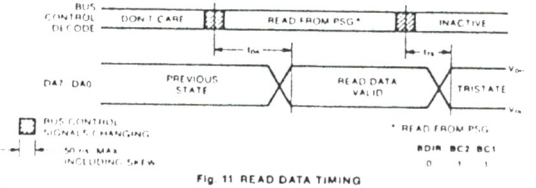


Fig. 11 READ DATA TIMING